Compensating Signal Generators for a Self-Calibrating Tracking Adc

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Abstract – This thesis introduces the possibilities of constructing of compensating signal generators for multi-bit self-calibrating tracking Analog-to-Digital Converter (ADC) on the basis of Digital-to-Analog Converter (DAC) with weight redundancy. In the paper we show that there are two possible approaches: with the construction of the digital part of the generator based on a purely binary system, and with the use of additional units based on the system of notation with weight redundancy. Under the proposed approach we consider the methods of structural and functional organization of the compensating signal generators on the basis of inaccurate DAC with weight redundancy.

***Index Terms* – Analog-digital conversion, calibration, digital circuits, digital control**

I. INTRODUCTION

Currently, the production and use of multi-bit tracking ADC has significantly decreased. With a decrease of tolerance of the analog hardware components parameters fitting the generating of the compensating analog signal faces discontinuities of the characteristics of transformation and thus decreases the accuracy of the analog to digital conversion.

The use of multi-bit binary DAC in tracking ADC to generate a compensating analog signal requires a significant amount of memory to generate a corrective amendment on each step of the transformation, which reduces the performance. However, implementation of the compensating signal generator (CSG) with the use of the DAC with weight redundancy (WR) simplify the procedure of generating of the compensating signal corrected values and significantly reduces the amount of memory required for this.

The aim of research is to analyze the feasibility of building a tracking ADC on the base of inaccurate analog components with the simplification of the self-calibration procedure, by insertion into its structure the CSG based on the DAC with WR.

Tracking ADC (Fig. 1b) belongs with a compensation type class (Fig. 1a) of the information form converters (IFC) and differs from others in relatively simple structure and a high rate of delivery of the output, because the output code is available for reading at each step of the conversion [1]. In such ADC an input analog signal (Ai) is balanced by the compensating analog signal (Ak), which is formed by the CSG included in the feedback loop.

Meanwhile, it is the digital equivalent $K(A_K)$ of the compensating signal Ak that is the result of the converting of the Ai:

$$K_{out} = K(A_K) \approx K(A_i).$$

Devices in Fig. 1 contain: C – a comparator, CSG – a compensating signal generator in the feedback loop, CU – a control unit, UDC – an up-down counter, DAC – a digital to analog converter, Nout – an output code, y_c –a comparator signal.

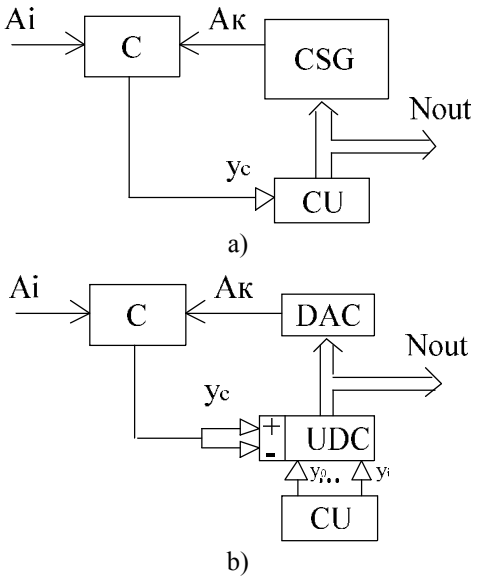

Fig. 1. Block diagrams of the compensation type ADC: a) generic; b) the tracking type.

It should be noted that the accuracy and the speed of setting of the Ak in compensation type ADC greatly affect the accuracy and the speed of the whole converter. The basic requirement for a generating of the Ak in tracking ADC is that the change of the Ak during one cycle of the approximation of the Ai does not exceed the value equal to the sum of the LSB and the minimum allowable static error.

Usually this requirement is met by means of correction of the instrumental errors of a DAC. At the same time, a bit resolution and a tolerable limit δQ of the ADC elemental base guidelines are crucial for the selection of the bit weights of the DAC correction method.

The authors proposed an approach to generating a compensating signal based on the use of a DAC with WR (α-DAC) in the CSG.

The main features of the DAC with WR are: continuity of its characteristic of transformation and the presence of the overlapping bands, which allows not only to maintain a given level of conversion errors due to self-calibration procedure but also to improve the accuracy of the ADC containing this DAC [2, 3]. Self-calibration is one of the self-correction procedures carried out by means of interruption of the basic transformation process for

determining actual bit weights values. The basic principle of the self-calibration procedure is that we divide n-bit converter's grid into a group of m "inaccurate" higher bits and "accurate" n-m lower bits (Fig. 2) [2]. Belonging to the "accurate" lower bits group is chosen from the condition that their absolute deviation does not exceed a half of the LSB:

$$\Delta Q_i \le 0{,}5 \cdot Q_0,$$

where Q_0 – analog value which corresponds to the weight of the IFC LSB.

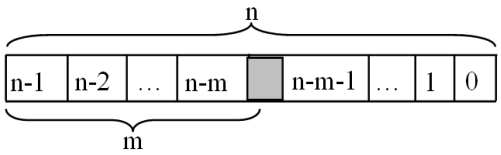

Fig. 2. The model of ADC's bit grid in self-calibration mode

II. THE METHOD OF A COMPENSATING SIGNAL GENERATING WITH THE INTERMEDIATE CONVERSION OF THE INPUT BINARY CODE INTO A CODE IN A REDUNDANT SYSTEM OF NOTATION

Generating of the Ak according to the current method can be divided into several stages.

During the first stage the self-calibrating procedure of the DAC with WR is performed. Self-calibration is used to determine the deviations of the higher "inaccurate" bits weights by comparing the weight of every such bit to the sum of the weights of a certain group of adjacent bits on the base of mathematical relations between them [3]. The result of the self-calibration procedure is the digital equivalents of the DAC real bit weights which are stored in a memory.

Such self-calibration results can be used repeatedly in the main conversion until the parameters of analog units of the CSG are changed due to changing of the temperature etc.

According to the current method a lookup table is used for generating of the Ak in a CSG. This table represents a set of pairs of codewords in a binary system N_i and corresponding codewords N_P in a redundant system of notation (RSN). To fill up this table the "digital equivalent - working code" converter and a binary counter are used (Fig. 3) [4].

An example of the lookup table for a CSG with 11-bit DAC with WR is shown in Table. 1.

To execute the procedure of a compensating signal generation according to the described method a CSG block diagram should contain the following components: a DAC with WR (α-DAC); an up-down binary counter (2-Counter), a storage (MEM) for a lookup table, a DC – memory cells address decoder.

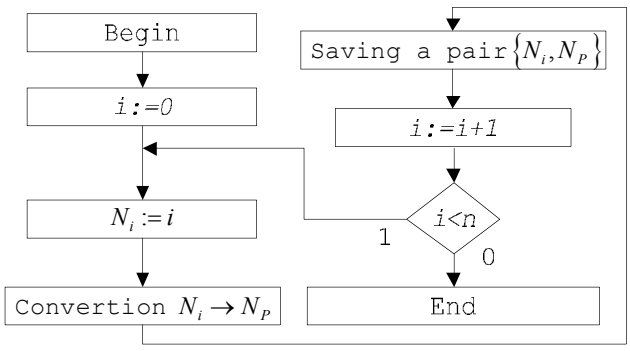

Fig. 3. Block diagram of filling up of the lookup table algorithm

TABLE 1. THE TABLE OF BOUNDARY CODEWORDS

i	N_i	N_P
0	00000000	00000000000
1	00000001	00000000001
2	00000010	00000000010
3	00000011	00000000100
4	00000100	00000000101
5	00000101	00000001000
6	00000110	00000001010
…	…	…

Block diagram of the CSG which uses the current method is shown in Fig. 4.

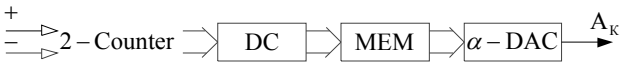

Fig. 4. Block diagram of a CSG

III. THE METHOD OF A COMPENSATING SIGNAL GENERATING WITH THE USE OF THE BOUNDARY CODEWORDS

Another method of a compensating analog signal generating with the use of a DAC with WR is based on the boundary codewords (BC). BC is an adjacent codes N_i' and N_i'' that differ in their analog equivalents by no more than the value of a LSB of the IFC. The presence of these codes is explained by the property of ambiguity of a number representation in RSN [2, 5].

For a BC the following condition is true:

$$A_i'' \le A_i' + Q_0,$$

where A_i'' – an analog equivalent of the N_i'' code, moreover:

$$A_i'' = \sum a_i \cdot Q_i,$$

where a_i – code N_i'' bit values, Q_i – IFC bit weights; A_i' – an analog equivalent of the code N_i', besides that:

$$A_i' = \sum a_i \cdot Q_i,$$

where a_i – code N_i' bit values.

Moreover, according to the proposed method of a compensating signal generating the counting (change of the codewords in a CSG counting device) "rule" can be described by the following expression:

$$N_{i+1} = \begin{cases} N_i', if\ N_i := N_i''; \\ N_i'', if\ N_i := N_i'. \end{cases}$$

where N_i and N_{i+1} – the current and the following code in the CSG counting device.

BC is searched only for the group of "inaccurate" bits. The search for each BC is carried out with the use of a successive approximation algorithm [1, 2], based on the approximation of the auxiliary analog signals A_{CAL} and $A_{CAL} + Q_0$ with and without switching on of the current bit and use of the recursion relations between the weights of the bits ($Q_i = Q_{i-1} + Q_{i-2} + ... + Q_{i-p-1}$) [2, 3, 5]. We obtain two codewords for each "inaccurate" bit (Table 2) as the result of this procedure.

TABLE 2. BOUNDARY CODE COMBINATIONS

Q_i	128,86	75,00	46,78	29,60	17,50	10,50	6,98	4,00	2,71	1,64	1,00	A_i	ΔA_i
N_i'	0	0	0	1	0	0	0	0	0	0	0	29,60	0,6
N_i''	0	0	0	0	1	1	0	0	0	0	1	29,00	

Here N_i' and N_i'' are the codes that define the BC. Block diagram of the BC search algorithm is shown in Fig. 5.

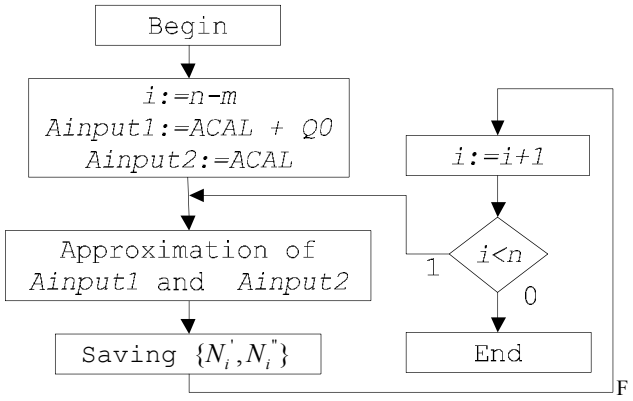

Fig. 5. Block diagram of the BC search algorithm

An example of the BC table for a CSG on the basis of 11-bit DAC with WR with the analog element base error limit level δQ =10% is shown in Table. 3. It should be noted that in this case of the DAC accurate and inaccurate groups should be divided so that n = 11, m = 7.

TABLE 3.THE TABLE OF BC

i	N_i'	N_i''
0	00000010001	000000011xx
1	00000100000	00000011xxx
2	00001000001	0000011xxxx
3	00010000000	000011xxxxx
4	00100000000	00011xxxxx
5	01000000001	0011xxxxxx
6	10000000001	011xxxxxxx

After analyzing the described above, a set of units that a CSG, which uses the proposed method of generation of the Ak should consist of, can be defined (Fig. 6). These are: a DAC with WR (α-DAC); an up-down counter in RNS (α-Counter), a storage for a BC (MEM), a digital comparison circuit (DCS) – to compare the current codeword and a BC, a selection of the BC sequence unit (SBCU).

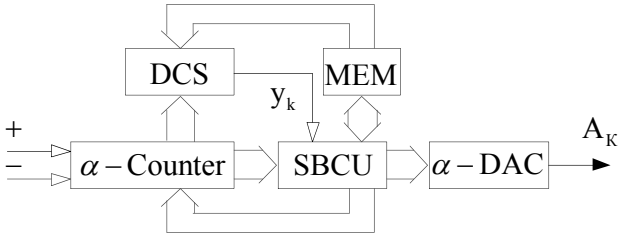

Fig. 6. A block diagram of the CSG with the use of a BC

IV. THE USE OF THE PROPOSED METHODS

The described schemes of the CSG can be used in a self-calibrating tracking ADC with imprecise analog elements. In Fig. 7 a block diagram of the ADC, which uses a CSG with BC is shown. Here: AS – an analogue switch; GCS – a generator of the calibration signal, RAM and ROM are short-term and read-only memory units, DCD – a digital computing device, SAR – a successive approximation register, Counter – a counter.

In Table. 4 and 5 the results of a computer simulation of the multi-bit tracking ADC with WR on the basis of the number system with a radix α=1,618, and an element base error limit level δQ =10% are shown.

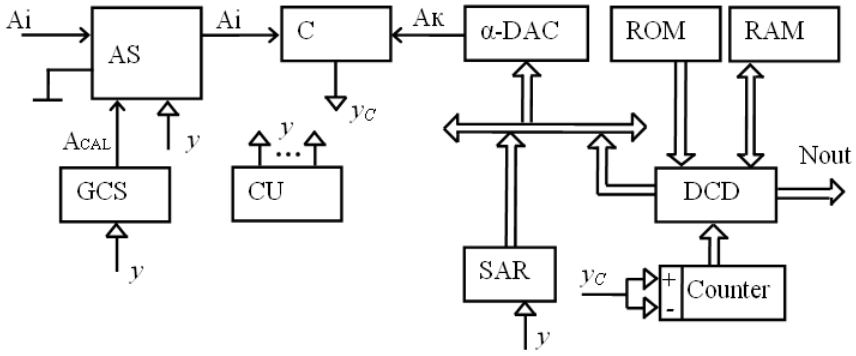

Fig. 7. A block diagram of the tracking ADC with WR, which uses the BC method

In Table. 4, 5 data in the columns numbered I, II, III are consistent with such methods of a compensating signal generating: without correction of the errors; based on the BC; with the intermediate conversion of the input binary code into a code in a redundant system of notation, respectively. Here, the integral and differential nonlinearity errors of the ADC built on inaccurate DAC, was calculated for 100 different sets of the DAC bit weights. In tables n_α and n_2 – the resolution of the DAC with WR and the resolution of the corresponding binary DAC respectively.

TABLE 4. INL STATISTICAL EVALUATION

Resolution (bits)	**M(INL)**	**σ(DNL)**

$n_2(n_\alpha)$	I	II	III	I	II	III
16 (23)	1375,07	7,63	2,014	867,58	0,82	0,43
14 (20)	300,72	6,14	1,76	188,72	0,65	0,35
12 (18)	115,21	5,26	1,62	60,77	0,52	0,32

TABLE 5. DNL STATISTICAL EVALUATION

Resolution (bits) $n_2(n_\alpha)$	M(INL)			σ(DNL)		
	I	II	III	I	II	III
16 (23)	698,14	1,95	1,27	524,35	0,24	0,21
14 (20)	211,39	1,91	1,23	101,92	0,18	0,17
12 (18)	62,56	1,92	1,19	47,26	0,15	0,17

Comparison of the proposed methods shows that the advantage of the method with the intermediate conversion of the input binary code into a code in a redundant system of notation is a higher accuracy. The disadvantages of this method are a large amount of memory needed for a lookup table and a large number of computations. While the advantages of the method based on the BC are a minor memory and computation requirements.

V. CONCLUSIONS

1. The possibilities of the construction of a multi-bit self-calibrating tracking ADC on the basis of the CSG with inaccurate DAC are analyzed. It is shown that there are two possible approaches: with the construction of the digital part of the CSG on the basis of a purely binary system and with the use of additional units based on the RNS.

2. Under the proposed approach, two methods of structural and functional organization of the CSG based on the inaccurate DAC were considered and simulated. The comparison of the proposed methods is given.

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