Low-Voltage Two NMOS IVB-Based Voltage-Mode First-Order All-Pass Filter With Tuning

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Abstract — In this paper, a new voltage-mode first-order all-pass filter suitable for low-voltage operation is presented. The circuit is composed of two n-channel metal-oxide semiconductor field effect transistors (NMOS)-based inverting voltage buffer (IVB), single capacitor, and three resistors. Replacing one of resistors by NMOS-based voltage-controlled resistor, the pole frequency of the filter can be controlled electronically. The theoretical results are verified by SPICE simulations using TSMC 0.13 μm level-7 CMOS process parameters, where ±0.65 V supply voltages of the IVB is used.

Index Terms — All-pass filter, analog signal processing, inverting voltage buffer, NMOS, voltage-mode circuit.

I. INTRODUCTION

First-order all-pass filters (APFs) are widely used to shift the phase of an input signal while keeping the amplitude constant over the frequency range of interest. Therefore, many current- or voltage-mode first-order APFs were designed and reported since 1966 [1]-[10]. The first voltage-mode (VM) APF was designed employing operational amplifier [1]. However, it suffers from the well-known limitations of opamp-based circuits such as frequency limitations and the use of a large number of passive elements. Therefore, to eliminate these disadvantages in APFs other types of active building blocks (ABBs) such as second-generation current conveyors (CCIIIs) [2], [3], third-generation current conveyors (CCIII) [4], [5], differential voltage current conveyors (DVCCs) [6], current differencing buffered amplifiers (CDBAs) [7], operational transconductance amplifiers (OTRAs) [8], or fully differential current conveyors (FDCCII) [9], [10], have started to be used. In general, above mentioned ABBs are unity-gain and non-tunable blocks. Hence, the change of the pole frequency by means of external DC bias current or voltage is not possible. Therefore, the electronically tunable APFs receive more attention nowadays, since the pole frequency of the circuits can be easily tuned. In the current technical literature the tunability is solved in three different ways:

i) the APF is designed using operational transconductance amplifier (OTA) [11], [12], or the internal structure of ABBs contains OTA [13], [14],

ii) by using current-controlled CCCI [15] or the input circuitry of ABBs allows to change the input intrinsic resistance [16], [17], or

iii) by replacing the appropriate floating/grounded resistor via voltage-controlled resistor (VCR) [18]-[20].

In addition, recently the research has started to focus on low-voltage and low-transistor count tunable APF design. The main goal of such circuits is of course, compared to above mentioned ABB-based counterparts, in the obtained lower chip area. As an example of such circuit the single inverting voltage buffer (IVB) with gain -1, three resistors, and one capacitor-based solution can be mentioned [21], which is in simulations implemented using internal structure of the inverting current conveyor. Another solution in [22] contains same number of passive elements, however, the IVB is realized in a more efficient way i.e. two n-channel metal-oxide semiconductor field effect transistors (NMOS transistors). In [23] a new approach for APF design was introduced, where instead of passive capacitors the gate-to-source capacitance (Cgs) of some MOS transistors are used. Due to the transconductance (gmn) of MOS transistors this design technique make the passive resistors unnecessary.

In this study, a new supplementary realization of VM APF employing single low-voltage IVB, three resistors, and single capacitor is presented. SPICE simulation results are included to support the theory. After replacing one of the resistors by NMOS-based VCR, the pole frequency of the filter is easily tuned in significantly much higher frequency range than it is demonstrated in [21] and [22], i.e. 7±11.5 MHz.

II. CIRCUIT DESCRIPTION

The proposed first-order VM APF is shown in Fig. 1. As it can be seen, circuit employs only two NMOS transistors realizing IVB with gain -1, single capacitor, and three resistors. Since only two NMOS transistors are between positive and negative supply voltages, the proposed circuit is suitable for low-voltage operation. Both transistors satisfy following conditions [24]:

\[ V_{GS} > V_{TN} \text{ and } V_{DS} > V_{GS} - V_{TN}, \]

hence they operate in saturation region.

The gain of the non-ideal IVB can be calculated as:

\[ A_i = \beta \frac{W_i}{L_i} \cdot \frac{1}{(W/L)_i}, \]

where \( \beta = 1 - \epsilon \). Here \( \epsilon \) (\( |\epsilon| \ll 1 \)) denotes voltage tracking error of the IVB and \( (W/L)_i \) (\( i = 1, 2 \)) is the channel width/length of the \( i \)-th transistor. Selecting equal
values for \( W/L \) of the transistors and considering precision design without error, an inverting voltage buffer with unity gain can be obtained.

The voltage transfer function (TF) of the proposed first-order APF shown in Fig. 1 is found as:

\[
T(s) = \frac{V_o}{V_i} = \frac{sCR_2R_{MOS}(2-\varepsilon_v) + R_2 - R_1(1-\varepsilon_v)}{sCR_{MOS}(2-\varepsilon_v)(R_1 + R_2) + R_1 + R_2}.
\]

Considering well designed IVB \((\varepsilon_v = 0)\) and selecting \(2R_1 = R_2\), the TF in Eq. (3) changes to:

\[
T(s) = \frac{V_o}{V_i} = \frac{1}{3} \frac{2sCR_{MOS} - 1}{2sCR_{MOS} + 1}.
\]

The phase response of the TF in Eq. (4) is calculated as:

\[
\phi(\omega) = 180^\circ - \arctg \left( 2\omega CR_{MOS} \right),
\]

and pole frequency \(f_0\) can be found as:

\[
f_0 = \frac{1}{4\pi CR_{MOS}},
\]

which clearly indicates that the \(f_0\) can be easily tuned by adjusting the value of \(R_{MOS}\).

By replacing the \(R_{MOS}\) via NMOS-based VCR working in triode region [20], as it is illustrated in Fig. 1, which resistance for low value of signal amplitudes can be calculated as \(R_{MOS} = L/\mu_nC_{OX}W(V_C - V_T)\), the pole frequency can be easily controlled via the DC control voltage \(V_C\). Here \(C_{OX}\) is the gate oxide capacitance per unit area, \(\mu_n\) is the electron mobility in the channel, and \(V_T\) is the threshold voltage of the transistor.

### III. SIMULATION RESULTS

To verify the theoretical study, the behavior of the proposed VM all-pass filter shown in Fig. 1 has been verified by SPICE simulations. In the design, transistors are modeled by the TSMC 0.13 \(\mu\)m level-7 CMOS process parameters \((V_{THN} = 0.04087 \text{ V}, \mu_n = 451.75678 \text{ cm}^2/(\text{V-s}), V_{THP} = -0.21787 \text{ V}, \mu_p = 100 \text{ cm}^2/(\text{V-s}), T_{OX} = 3.2 \text{ nm})\) [25]. The DC power supply voltages are equal to \(V_{DD} = -V_{SS} = 0.65 \text{ V}\). The aspect ratios of IVB MOS transistors \(M_1\) and \(M_2\) were chosen sufficiently high \(W/L = 78 \mu\text{m}/0.26 \mu\text{m}\) to decrease the loading effect. In the frequency range of our interest the beta \(\beta\) can be assumed to be constant with value \(1 - \varepsilon_v = 0.939\) and its \(f_{3dB}\) frequency is found to be 114.39 GHz. In the simulations, the value of the capacitor \(C\) was selected as 2 pF and the resistors \(R_{MOS} = R_1 = 4 \text{ k}\Omega, R_2 = 2 \text{ k}\Omega\), which results in a 90\(^\circ\) phase shift at \(f_0 \approx 8.9 \text{ MHz}\). The ideal and simulated gain and phase responses of the proposed filter is shown in Fig. 2(a). Note that the obtained \(f_0\) is equal to theoretical one. Time-domain simulation result of the proposed filter is shown in Fig. 2(b) in which a sine-wave input of 100 mV amplitude and frequency of 8.9 MHz was applied to the filter while keeping the passive element values as listed above. Since

![Fig. 1. Proposed voltage-mode two NMOS-based all-pass filter.](image1)

![Fig. 2. (a) Ideal and simulated gain and phase characteristics of the proposed VM APF, (b) time-domain responses at 8.9 MHz, (c) Lissajous pattern showing 90\(^\circ\) phase shift at pole frequency.](image2)
the gain of the proposed filter is 1/3, the amplitude of the output voltage is decreased accordingly. The total harmonic distortion at this frequency found as 1.107%. In addition, the 90° phase shift in the output with the input (at pole frequency) is also illustrated in the Lissajous pattern shown in Fig. 2(c). To illustrate the electronic tunability of the proposed filter, the resistor $R_{\text{MOS}}$ was replaced by NMOS-based VCR, as it is demonstrated in Fig. 1. The $W/Z$ ratio for the $M_k$ is chosen as 2.47 $\mu$m/1.3 $\mu$m. The pole frequency is varied for $f_0 \approx \{7; 8.9; 11.5\}$ MHz via $V_C = \{0.43; 0.48; 0.56\}$ V, respectively.

IV. CONCLUSION
This paper presented low-voltage and low-transistor count first-order VM APF, which good workability was proved by SPICE simulations. Compared to circuits in [4] and [8], where respectively 24 and 20 transistors are used in the structure of ABBs, in this paper the inverting voltage buffer contains only two NMOS transistors. Moreover, the pole frequency can be easily tuned.

Future work will be focused on cascadable low-transistor count VM circuit design features with high-input and/or low-output impedances.

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