High Performance Wideband CMOS CCI with High Voltage Swing

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***Abstract* —In this study, low-voltage, high performance and wideband CMOS first generation current conveyor (CCI) is proposed. The proposed CCI has very low equivalent impedance on port X. It also has high voltage swings on input and output ports and wideband current and voltage transfer ratios. Furthermore, two novel grounded inductance simulator circuits are proposed as application examples. It is shown that the simulation results are in very good agreement with the expected ones.**

***Index Terms* — CCI, first generation current conveyor, low-voltage.**

I. INTRODUCTION

In this study, an accurate CMOS CCI implementation is proposed. The presented CCI has very low parasitic resistance in series to port X due to super source follower feedback configuration. The proposed circuit has high voltage swings on input and output ports and wideband current and voltage transfer ratios. Moreover, two grounded inductance simulator circuits are presented as application examples. The behavior of physical inductors cannot be close to ideal component behavior in comparison to resistors and capacitors and in terms of spatial dimensions. They are larger than the other circuit elements, if the inductance value is not sufficiently small. Actively simulated inductors find application areas like oscillators and active filter design problems. For this reason, there are many publications on the active simulation of inductances [1-14]. Different current-mode active elements are used in the design of inductance simulator circuit such as current conveyor [1], negative impedance converter [4], current feedback operational amplifier [5-6]. Although CCI is the firstly proposed current conveyor introduced in 1968 [7], it has not found enough application areas in the design of the inductance simulators except [8]. Therefore, two supplementary inductance simulators are presented with CCI in addition to a novel CMOS CCI implementation. HSpice simulations are performed to verify the theory.

II. THE PROPOSED CMOS CCI

CCI is a three terminal active device which ensures two functionalities between its terminals. The voltage applied to Y port is copied to X port and the current flowing through X port is copied to Y and Z ports all with unity gains. The port relations of a CCI can be described by the following equation:

$$V_X=\beta V_Y, \qquad I_Y=\gamma I_X, \quad I_Z=\alpha I_X \tag{1}$$

where β, α, and γ are unity for an ideal CCI and they represent the voltage and current transfer gains, where all currents flow into the device.

The proposed CMOS CCI depends on differential pairs to provide high voltage swings on ports X and Y. The operation of the circuit can be explained as follows: Transistors M13 and M14 provide DC biasing currents for the differential pairs. Active load transistors M9-M12 force equal currents to source coupled transistors M1-M4 and as a result gate-to-source voltages of M1, M4 and M2, M3 have equal values, $v_{gs1}=v_{gs4}$ and $v_{gs2}=v_{gs3}$. This operation allows the voltage at output port to follow the voltage at input port.

The CCI employs two source followers, M_6 and M_7, to obtain low equivalent impedance at X port. A well known method to reduce the impedance is to use feedback. This technique can be conveniently applied to the source followers M6 and M7. When local feedback is applied to the source follower transistors improved output stages can be obtained. These new configurations are called super source followers [9] and they are shown in Fig. 1a. The gain stage amplifies the difference between the input and output of the source follower, thus reducing the output impedance by the amplification factor of the gain stage itself. The improved differential pair based CMOS CCI that employs super source followers is shown in Fig. 1b. Just like the conventional source follower, the input signal is replicated

at the sources of M6 and M7, but it is also amplified at the drains of same transistors. The amplified signal is fed to the inputs of M_{15} and M_{16} which operate as the input elements of the second gain stage [9]. Feedback loops are thus established through transistors M7, M16 and M6, M15. With the improved configuration, the equivalent resistance on port X is equal to:

$$R_x = \frac{1}{g_{m11}g_{m14}r_o(1+g_{m10}r_o/2)} \Big\| \frac{1}{g_{m12}g_{m15}r_o(1+g_{m9}r_o/2)} \quad (2)$$

The β parameter of the proposed CCI can be easily derived and it is equal to:

$$\beta \cong \frac{v_X}{v_Y} = \frac{g_{m7,8}}{g_{m9,10}} \quad (3)$$

Transistors with large output resistances are required to obtain a β value that depends only on the input pair transconductance ratios. The β parameter is given by the transconductance ratios of the input transistors, so it is very close to the ideal unitary value.

Transistors M16 and M17 are used to sense the current flowing through X port and copy it to the high-impedance Z port. The equivalent resistance seen on port Z is equal to:

$$R_Z \cong \frac{r_{o16}r_{o17}}{r_{o16}+r_{o17}} \quad (4)$$

The α parameter of the CCI is equal to:

$$\alpha \cong \frac{i_Z}{i_X} = \frac{g_{m16,17}}{g_{m14,15}} \quad (5)$$

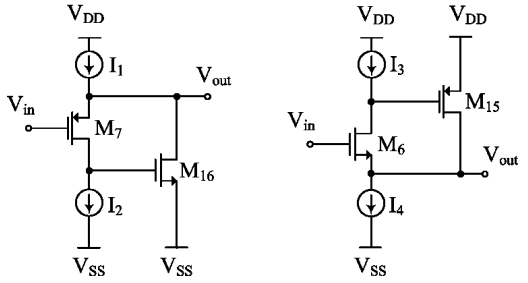
If the load impedance connected to high impedance port Z is negligible with respect to the transistor output resistances, the α parameter can be given by the transconductance ratios of the current mirror transistors and it is very close to the ideal unitary value.

Transistors M18 and M19 are used to copy the current flowing through X port to high impedance Y port. The equivalent resistance seen on port Y is equal to:

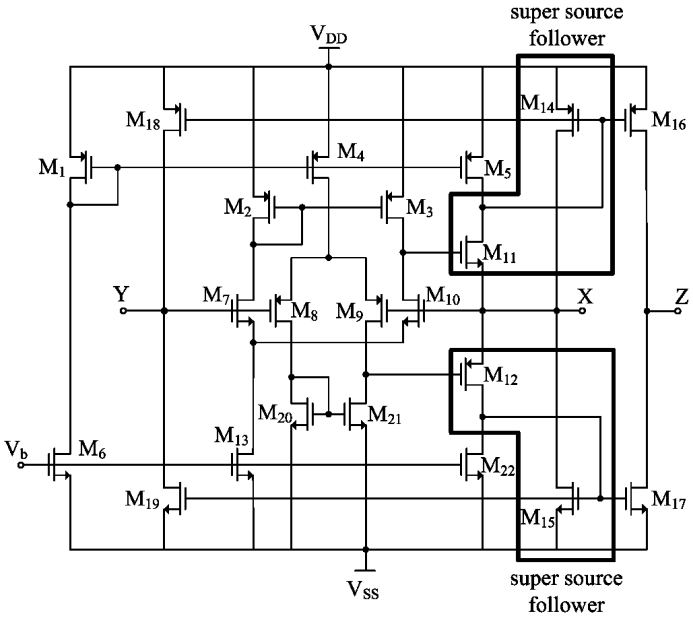
$$R_Y \cong \frac{r_{o18}r_{o19}}{r_{o18}+r_{o19}} \quad (6)$$

Similar to (5), the γ parameter can be calculated as:

$$\gamma \cong \frac{i_Y}{i_X} = \frac{g_{m18,19}}{g_{m14,15}} \quad (7)$$



(a)



(b)

Fig. 1. (a) Super source follower configurations (b) The proposed high performance CMOS CCI

III. APPLICATION EXAMPLE: THE PROPOSED INDUCTANCE SIMULATOR CIRCUITS

The proposed grounded inductance topologies are given in Fig. 2. The circuit in Fig. 2b employs a voltage buffer [9]. For the proposed circuit in Fig. 2a, the following input impedance function is obtained for the matching conditions of G_1=3G, G_2=G_4=2G and G_3=G,

$$Z_L = \frac{sC}{10G^2} \quad (8)$$

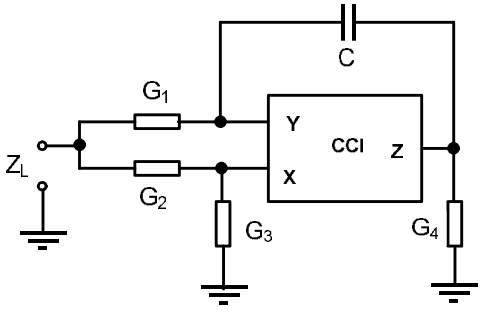
The impedance transfer function for the circuit in Fig. 2b is equal to:

$$Z_L = \frac{G_1+G_2+sC}{G_1G_2} \quad (9)$$

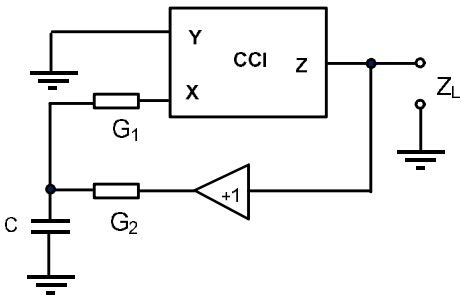
Taking the non-ideal affects into consideration, the input impedance functions of the inductance simulators in Fig.'s 2a and 2b will be respectively equal to:

$$Z_L = \frac{12G(\beta-\gamma)+sC(10\beta-6\gamma-6\alpha)}{4G^2(6\gamma\beta+6\beta-11\gamma-6)+2sCG(6\alpha\beta+6\gamma\beta+16\beta-11\alpha-11\gamma-6)} \quad (10)$$

$$Z_L = \frac{V_{in}}{I_{in}} = \frac{G_1+G_2+sC}{\alpha\beta G_1G_2} \quad (11)$$



(a)



(b)

Fig. 2. The proposed inductance simulator circuits (a) lossless one (b) lossy one

IV. SIMULATION RESULTS

The aspect ratios of the transistors are selected as: 30µm/0.5µm for M1 and M5, 10µm/0.5µm for M6, 20µm/0.5µm for M7, M10, M13 and M22, 60µm/0.5µm for M4, M8 and M9, 60µm/0.35µm for M2 and M3, 10µm/0.35µm for M15, M17 and M19, 20µm/0.35µm for M20 and M21, 30µm/0.35µm for M11, M14, M16 and M18 and finally 90µm/0.35µm for M12.

The simulation results of the equivalent impedance on port X is given in Fig. 3a. Its value is only 2.5Ω at 1MHz, 7.1Ω at 10MHz and 100.0Ω at 100MHz. Port Z impedance value is about 132kΩ at low frequencies and its value decreases as the frequency increases. Its value is about 122kΩ at 10MHz and 35kΩ at 100MHz. It is seen that the impedance values of the proposed CCI are very similar to the ideal CCI values in a wide frequency range.

In Fig. 3.b the linear operation region of the voltage follower stage is given for the ideal CCI, the proposed CCI and the difference between the two. The proposed circuit

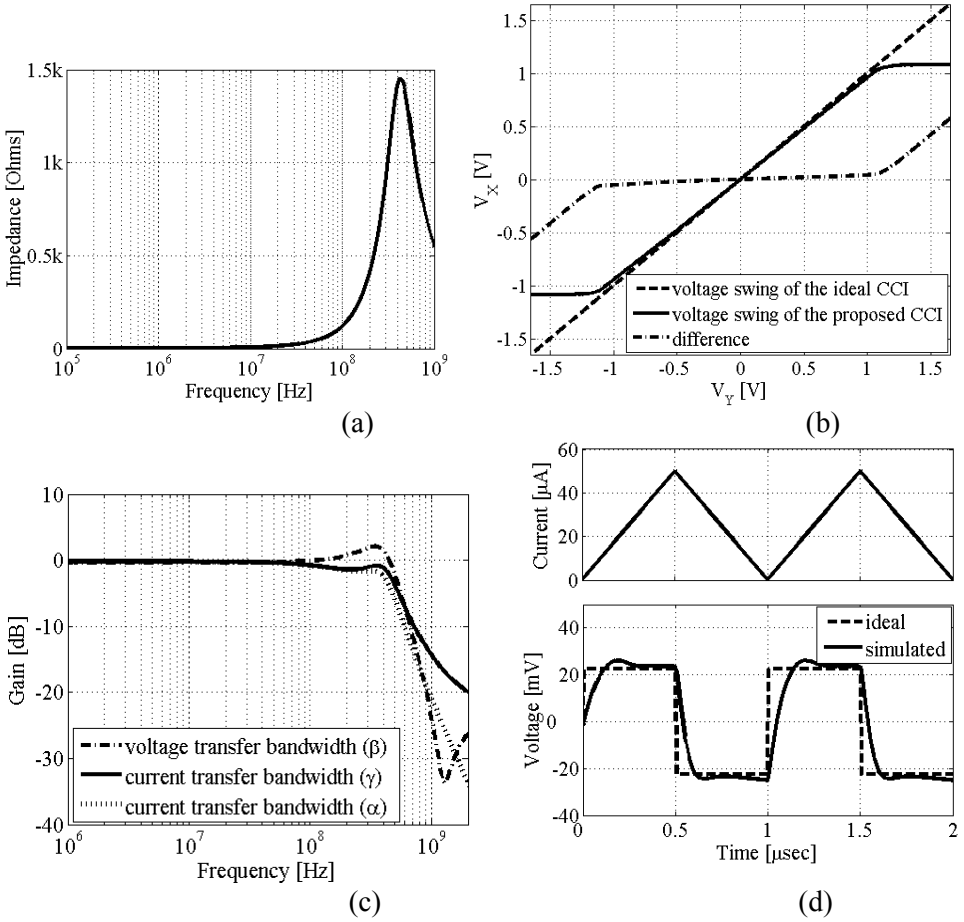


Fig. 3. (a) Variation of port X impedance value with frequency (b) Linear operation region of the proposed CMOS CCI (c) Current and voltage transfer gains (d) Time domain simulation results of the proposed lossless grounded inductance simulator

has a linear voltage swing between ±1.1V with less than ±6% error.

The current and voltage transfer ratios, α, γ and β, are found to be 0.99, 0.99 and 0.98, respectively. 430MHz current transfer bandwidth from port X to port Z, 480MHz current transfer bandwidth from port X to port Y and 570MHz voltage transfer bandwidth from port Y to port X are obtained as given in Fig. 3c with about 683µW power consumption.

The functionality of the proposed lossless grounded inductance simulator circuit given in Fig. 2.a is tested both in time and frequency-domain. Time-domain functionality of the circuit is illustrated with element values R_1=1kΩ, R_2=1.5kΩ, R_3=3kΩ, R_4=1.5kΩ, and C=0.5nF to obtain an inductor of value 225µH. A triangular current signal of 50µA peak value is applied to the inductor. Also an equal current is applied to an ideal passive inductor. The input current and the ideal/simulated inductor voltages are shown in Fig. 3.d. The inductor voltage is a square wave with 22.5mV peak value where $V_L = L_{eq}\, dI_L/dt$.

CONCLUSION

In this paper, differential pair based high performance wideband CMOS CCI is proposed. Moreover, two novel grounded inductance simulators that employ a single CCI are also given as an application example. It is shown that the simulation results are in very good agreement with the expected ones.

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