Multidimensional Digital Signal Processing for Printed Circuit Boards Testing

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Abstract — A new method for multidimensional digital signal processing for Printed Circuit Boards (PCB) testing is described. The considered method comes to solve such problems as competition and synchronization, which are present in the multidimensional signals processing. The solution is achieved by performing in parallel all operations, replacing the analog-to-digital conversion (ADC) with differentiation operations and analyzing the signal variation rate based on the Fuzzy logic elements. As a result of these operations, using digital integration models, binary code streams are obtained that allow the reconstruction of the signal shape. Mathematical models applied for the transformation and processing of multidimensional signals are presented. The designed system for the multidimensional signal processing consists of a computing unit, the test signals generator, the data storage unit, the Printed Circuit Board with nodes for test signals application and retrieval, and finally the processing elements for differentiation and analysis based on Fuzzy logic.

Keywords — multidimensional signal, digital signal processing, PCBs testing, Fuzzy logic, FPGA, ADC.

I. INTRODUCTION

Multidimensional signals are present in all aspects of our lives. Because of the immense relevance of signal processing and the fast-growing requirements of industry and business, the most important topics in this domain are signal processing analysis and architectures design. Currently, a lot of mathematical methods and models are developed for multidimensional signal processing with applications in various fields, such as medicine (2D and 3D image processing), industry (Multi-Input Multi-Output systems), economics and management (Data Mining, OLAP), etc.

From a mathematical point of view, any process can be defined in a multidimensional space with an absolute or relative coordinate system through a lot of variables depending on the coordinate system [1, 2, and 3].

An important area for the application of multidimensional signal processing methods and models can be considered the Printed Circuit Boards (PCB) functional and parametric testing. In this case, the PCB can be considered as a Multi-Input Multi-Output system that evaluates in a 2D space, if the board has a one-layer conductive pattern, and 3D, if the board is multi-layer [4, 5, and 6].

The PCBs testing requires a complex multilateral approach that ensures the identification of hardware defects at the topology and logical levels and those at the level of dynamic and transient processes. All these operations can be performed sequentially, with limited resources and at a low cost, or in parallel, using a complex and very expensive systems.

Dynamic and transient processes that occur in PCBs are concurrent processes that require the generation of multiple test signals at the same time with the acquisition of another set of state signals that determine the result of signals-propagation in PCB conductors.

Therefore, the notion of concurrency for PCBs testing is a decisive factor that will determine the correctness of this operation. Respectively, having a Printed Circuit Board with N test nodes also requires N analog-to-digital converters with very high frequency to ensure the detection of delays and transient processes.

In [7, 8] the method of system synthesis for parallel multidimensional signals acquisition and processing for performing the Printed Circuit Boards testing is described. The system contains a lot of homogeneous input channels that perform in parallel data acquisition.

Methods of modeling and synthesis of PCBs testing systems based on Hardware Petri nets implemented into FPGA circuits are described in [9, 10]. The application of Hardware Petri nets models for PCBs testing ensures the validation of the testing system before it is implemented in reconfigurable circuits.

In this paper, a method for digital processing of multidimensional signals for Printed Circuit Boards testing is proposed. The method ensures the simultaneous generation of input signals on the board, the acquisition and concurrent processing of test signals, excluding the analog-to-digital conversion.

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II. Problem Statement

Let's consider a Printed Circuit Board (Figure 1) with: a set of nodes $U^{In} = \{u_i^{In}, \forall i = \overline{1,N}\}$, $(N = 7)$, that represents the input signal vector; a set of nodes $U^{Out} = \{u_j^{Out}, \forall j = \overline{1,K}\}$, $(K = 8)$ that denotes the vector of functional and parametric test signals, where the analytical model for U^{Out} signal calculation is defined as $u_j^{Out} = g_j(U^{In}, Z_j)$; the matrix of electrical impedances generated by the respective conductors $Z = [Z_{i,j}, \forall i = \overline{1,N}, j = \overline{1,K}]$, where $Z_{i,j} = f_{i,j}(R_{i,j}, L_{i,j}, C_{i,j}), \forall i = \overline{1,N}, j = \overline{1,K}$, $f_{i,j}$ is the calculation formula in which $R_{i,j}$ represents the electrical resistance of the conductor, $L_{i,j}$ is the conductor inductance and $C_{i,j}$ is the electrical capacity of the conductor.

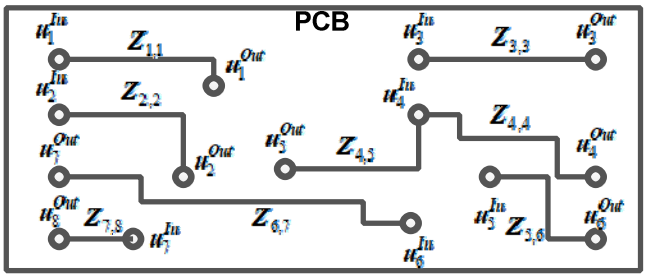

Fig. 1. Printed Circuit Board.

In our research, we propose to develop a system that allows PCBs testing using input signal U^{In} generation models, concurrent acquisition of multidimensional output signals U^{Out} and their digital processing to identify the influence of the electrical signal propagation process in the conductors and their mutual influence.

III. Functional Block Diagram of the System

Figure 2 shows the functional block diagram of the system for Printed Circuit Board testing based on the digital processing of multidimensional signals.

The functional block diagram consists of: a computing unit ***PC*** that contains the environment for the development and programming FPGA circuits and the tool for multidimensional signals digital processing; ***FPGA TSG*** - FPGA circuit configured according to test signal generator (vector U^{In}); ***PCB*** - Printed Circuit Board to be tested, with inputs U^{In} and outputs U^{Out}; du_j^{Out}/dt - elements of time differentiation, calculate the speed of signals variation at the PCB outputs (vector U^{Out}); $A\dot{U}^{Out}$ - amplification elements and Fuzzy logic units that encode the speed of output signal variation and generate a binary code Y; ***FPGA SAP*** - FPGA circuit configured according to data stack and interface for data transfer to ***PC***; ***SYN*** - synchronization block of the data storage process.

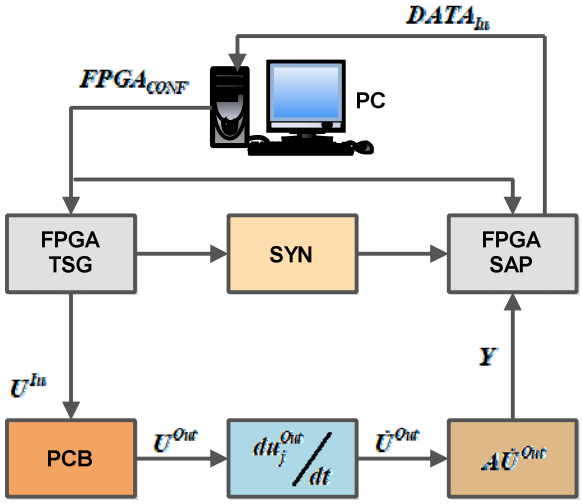

Fig. 2. Functional block diagram.

IV. Fuzzy Logic Unit Block Diagram

The functional block diagram of the Fuzzy logic unit is presented in Figure 3.

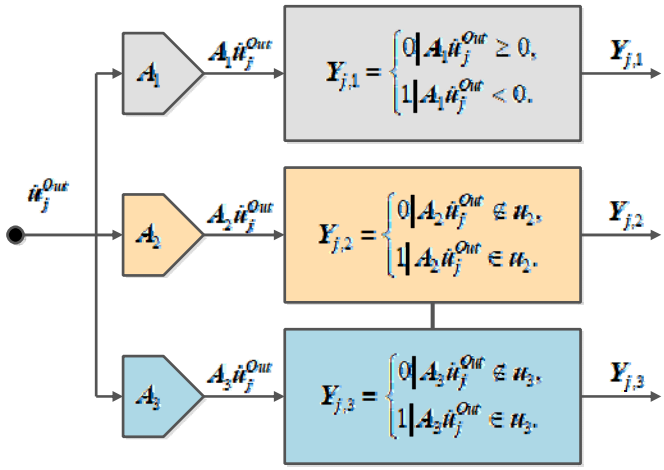

Fig. 3. Fuzzy logic unit block diagram.

The Fuzzy logic unit transforms the variation speed and polarity of the output signal $\dot{u}_j^{Out}$ into binary code. The set of amplifiers $A_1, \ldots A_3$ boosts the $\dot{u}_j^{Out}$ signal level to the analysis level $A_l \dot{u}_j^{Out}, \forall l = \overline{1,3}$. The bit $Y_{j,1}$ determines the sign of the binary code (positive – 0 and negative - 1). The bits $Y_{j,2}$ and $Y_{j,3}$ represents the binary code of the output signal speed variation.

Depending on the working frequency of the Printed Circuit Board, the sampling step for the Fuzzy logic is calculated. Table I presents the approximation codes.

Here $\dot{u}_j^{Out} = du_j^{Out} / dt$ is the speed variation of the output signal; $Y_{j,1}$, $Y_{j,2}$, $Y_{j,3}$ - approximation binary code; $\Delta\dot{u}$ - the discretization step.

TABLE I. APPROXIMATION CODES

No.	$\dot{u}_j^{Out}$	$Y_{j,1}$, $Y_{j,2}$, $Y_{j,3}$
1.	$0 \le \dot{u}_j^{Out} < \Delta\dot{u}$	000
2.	$\Delta\dot{u} \le \dot{u}_j^{Out} < 2\Delta\dot{u}$	001
3.	$2\Delta\dot{u} \le \dot{u}_j^{Out} < 3\Delta\dot{u}$	010
4.	$3\Delta\dot{u} \le \dot{u}_j^{Out} < 4\Delta\dot{u}$	011
5.	$0 < \dot{u}_j^{Out} < -\Delta\dot{u}$	100
6.	$-\Delta\dot{u} \le \dot{u}_j^{Out} < -2\Delta\dot{u}$	101
7.	$-2\Delta\dot{u} \le \dot{u}_j^{Out} < -3\Delta\dot{u}$	110
8.	$-3\Delta\dot{u} \le \dot{u}_j^{Out} < -4\Delta\dot{u}$	111

Figure 4 shows the models of signal shape and the connection with the approximation codes.

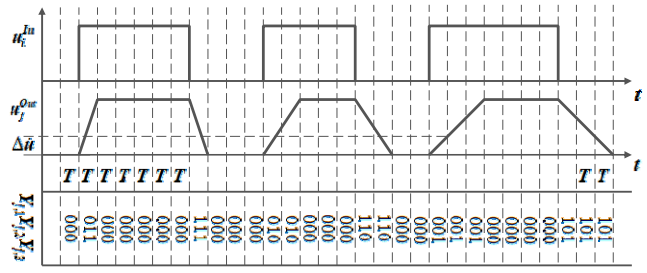

Fig. 4. Generation of approximation codes.

The sequences of the approximation codes are stored in the stack memory configured on the ***FPGA SAP*** circuit. The data from the stack memory is transmitted to the computing unit ***PC*** .

In order to test the mathematical models that determine the functionality of the Fuzzy logic unit, an AHDL code that realizes the approximation codes defined in Table I was written. The validation of the AHDL code was performed in the IDE Quartus Prime 19.1 development environment [11]. The simulatin results are shown in Figure 5.

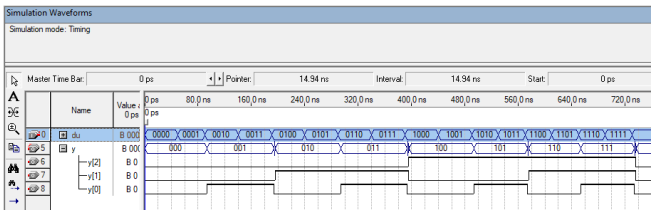

Fig. 5. Simulation results for the Fuzzy logic unit.

V. MATHEMATICAL MODELS FOR DATA PROCESSING

The functional correctness of the Printed Circuit Board is determined as a result of processing the data acquired from the output nodes U^{Out}. These data processing operations are performed by the computing unit ***PC*** .

Three mathematical models are provided for these operations:

1. Reconstitution of the acquired signals model;
2. Influence of the PCB topology on the output signals model;
3. Mutual influence of the output signals model.

A. Reconstitution of the acquired signals model

The reconstruction of the acquired signal shapes is performed based on the model (1), where: n is the number of the signal reconstruction step; T is the sampling step that is equivalent to dt ; $Y_{j,i} \forall j = \overline{1,K}, i = \overline{1,3}$ is the binary code for evaluation of the reconstituted signal variation rate; $\Delta\dot{u}$ is the discretization step.

$$U^{Out}(nT) = \begin{bmatrix} \sum_0^n \left(\left(Y_{1,1} Y_{1,2} Y_{1,3} \right)_n \times \Delta\dot{u} \right) \\ \sum_0^n \left(\left(Y_{2,1} Y_{2,2} Y_{2,3} \right)_n \times \Delta\dot{u} \right) \\ \dots \\ \sum_0^n \left(\left(Y_{K,1} Y_{K,2} Y_{K,3} \right)_n \times \Delta\dot{u} \right) \end{bmatrix}, n = 0,1,2,... \quad (1)$$

As a result of the signal reconstruction, approximation models in a continuous space will be obtained. This will allow the extraction of the functional and parametric status information from the PCB.

B. Influence of the PCB topology on the output signals model

To describe the influence of the PCB topology on the output signals, the mathematical model (2) is proposed:

$$F\left(\frac{U^{Out}}{U^{In}}\right) = \begin{bmatrix} \frac{\partial u_1^{Out}}{\partial u_1^{In}} & \dots & \frac{\partial u_K^{Out}}{\partial u_1^{In}} \\ \dots & \dots & \dots \\ \frac{\partial u_1^{Out}}{\partial u_N^{In}} & \dots & \frac{\partial u_K^{Out}}{\partial u_N^{In}} \end{bmatrix}. \quad (2)$$

This model highlights the influence of the input signals on all output signals. In this way, the apparent capacitive and inductive connections between two conductors can be identified. By concurrent and simultaneous generation of the input signals in the test nodes and by parallel signals

acquisition from all output nodes, it is possible to identify errors in the design process or the technological process of PCBs fabrication.

For the mathematical model (2) the N dimension coordinate system is defined, where N represents the number of nodes for input signal acquisition (the vector U^{In}). In the PCBs testing process, K variables will be analyzed, which represents the number of nodes for the output signals (the vector U^{Out}).

The following expression is defined for each output signal:

$$F\left(U_j^{Out}\right) = f_j\left(U_i^{In}, \forall i = \overline{1,N}, t\right)$$

C. Mutual influence of the output signals model

Useful information for PCBs testing can also be obtained as a result of analyzing the mutual influence of the output signals, applying the mathematical model (3):

$$F\left(\frac{U^{Out}}{U^{Out}}\right) = \begin{bmatrix} \frac{\partial u_1^{Out}}{\partial u_1^{Out}} & \cdots & \frac{\partial u_K^{Out}}{\partial u_1^{Out}} \\ \cdots & \cdots & \cdots \\ \frac{\partial u_1^{Out}}{\partial u_K^{Out}} & \cdots & \frac{\partial u_K^{Out}}{\partial u_K^{Out}} \end{bmatrix}. \quad (3)$$

The mathematical model (3) offers the possibility to obtain a set of correlation functions that characterize the dynamics of the output signals U^{Out}.

VI. CONCLUSIONS

The electronics and systems manufacturing industry require new methods and technologies for the functional and parametric PCBs testing. The complexity of these systems is obvious, as it is necessary to perform several parallel and concurrent operations, which include test signals generation and state signals acquisition from the tested PCB. The most complex and expensive operation is the acquisition of signals that also include analog-to-digital conversion. In this way, the PCBs testing can be considered a digital processing of the multidimensional signals.

In this paper, a new PCBs testing method is described that excludes the analog-to-digital conversion operation of the analyzed signals. This approach allows to reduce the complexity and cost of the signal acquisition elements. The use of FPGA circuits for the implementation of the test signal generator and the stack for data storage ensures greater flexibility and the possibility to apply design methods based on Hardware Petri net models.

The proposed method is based on the differentiation of the analyzed signals, the identification of the variation speed and its approximation with a binary code (1 bit for sign and 2 bits for data). Fuzzy logic elements are used for the approximation operation.

For the future, further research will be conducted in the functional and parametric validation of the PCBs testing system and evaluation of different types of errors during the testing process, depending on the sampling frequency, the number of bits in the approximation code, the maximum frequency of the input signals, etc.

ACKNOWLEDGMENT

The research carried out in this paper is part of the research activity of the Department of Computer Science and Systems Engineering, Technical University of Moldova. The validation of the proposed models was carried out with the support provided by the laboratory "Designing and Modeling Systems" and within ICG Engineering SRL, R. Moldova.

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