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THE IMPLEMENTING OF NONLINEAR MATHEMATICAL FUNCTIONS USING LOG-DOMAIN CIRCUITS

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Abstract. *In this paper the design of various nonlinear functions, like dividers, n^{th} order rooters and exponentiations blocks, using log-domain circuits is presented. The circuits consist of simple exponential and logarithmic cells, designed in bipolar technology. An important advantage of the proposed structures is that they are current mode operating circuits, having an extended dynamic range and a good frequency response. The 0.8 µm BiCMOS technology simulations confirm the theoretical results.*
Keywords: *nonlinear function, log-domain circuits, divider, square-rooter, exponentiation, transconductor.*

Introduction

Analog signal processing circuits continue to receive significant attention. Analog circuits that realize various nonlinear functions are important building blocks in many applications.
Various methods used for implementing non-linear mathematical functions are presented in the literature [1] – [4]. Among these, the most difficult is to realize the divider, requesting high complexity circuits which are difficult to implement in silicon [3].
In this paper a new method for implementing usual non-linear mathematical functions by using log-domain circuits is presented. The resulted structures are current mode operating circuits, having an extended dynamic range and a good frequency response. These circuits consist of a current to voltage converter at the input, having a non-linear transfer function f_1^{-1} (of logarithmic type) and a voltage to current converter to the output, having also a non-linear transfer function f_2 (of exponential type), chosen so that the two non-linearities cancel each other and so resulting the wanted mathematical function.
One of the simplest applications of these circuits is the linear current amplifier.
Other applications of these structures are the ELIN (externally linear, internally nonlinear) circuits that can implement any type of transfer function, so resulting linear structures with an also extended dynamic range.
As an application of this technique, in this paper is presented a new method for implementing the divider, the n^{th} order rooter and the raising to a power operation made by exponential and log-domain non-linear circuits.

2. The Linear Current Amplifier Principle

In Fig. 1 is presented the principle of a linear current amplifier by compensation of the input and output transconductors stages nonlinearities.

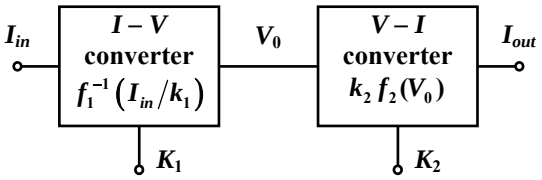

Fig. 1. Current mode amplifier using two nonlinear

The input stage is a current to voltage converter (***CVC***) described by the following equation:

$$V_0 = f_1^{-1}\left(\frac{I_{in}}{k_1}\right) \tag{1}$$

From equation (1), the I_{in} current can be expressed as:

$$I_{in} = k_1 f_1(V_0) \tag{2}$$

The output stage is a voltage to current converter (***VCC***), described by the following equation:

$$I_{out} = k_2 f_2(V_0) \tag{3}$$

If the two transconductor stages are chosen so that:

$$f_1 = f_2 = f \tag{4}$$

then, from (2) and (3) it results that:

$$\frac{I_{out}}{I_{in}} = \frac{k_2}{k_1} \tag{5}$$

For a practical implementation, the coefficients k_1 and k_2 are the bias currents of the two transconductors stages and the function f may be of various types as: exp, tanh, sinh.

In the following, we will use the principle of nonlinearities compensation (seen above) to implement the different nonlinear functions using log-domain circuits, where f is an exponential function.

3. Logarithmic and Exponential Type Basic Cells

By using the logarithmic type circuits, one can easily implement the expanding (exponential type) and compressing (logarithmic type) functions, necessary in many applications. In Fig. 2 a first possibility for implementing of these functions is presented. All transistors are considered perfectly matched and the base current has been neglected.

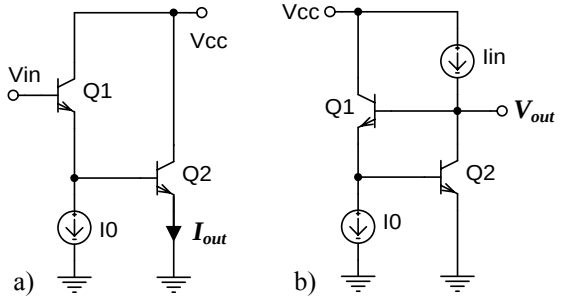

Fig. 2. a) Expanding cell (exp)
b) Compressing cell (log)

The circuit in Fig. 2.a) realizes the exponential type expanding functions, described by the following mathematical relation:

$$I_{out} = \frac{I_S^2}{I_0} \cdot \exp\left(\frac{V_{in}}{V_T}\right) \tag{6}$$

The circuit in Fig. 2.b) realizes the logarithmic type compression functions, described by the following relation:

$$V_{out} = V_T \ln\left(\frac{I_0}{I_S^2} I_{in}\right) \tag{7}$$

In (6) and (7), I_S is the saturation current considered equal for all the transistors and $V_T = 26\,\text{mV}$ is the thermal voltage.

In Fig. 3 an other exponential type expanding cell is presented.

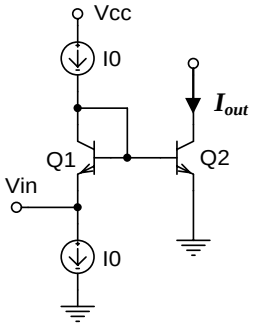

Fig. 3. Expanding cell (exp)

It is described by the following mathematical relation:

$$I_{out} = I_0 \exp\left(\frac{V_{in}}{V_T}\right) \tag{8}$$

In Fig. 4.a) and b) a differential stage expanding

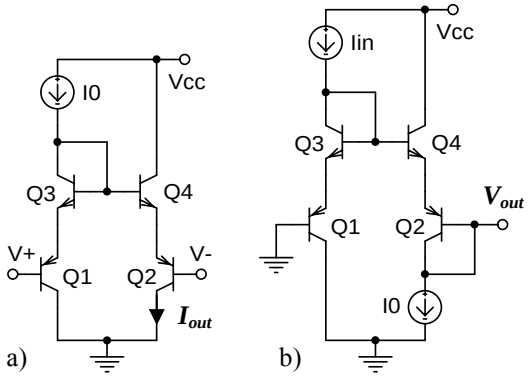

Fig. 4. Differential expanding cell (a) and correspondent compressing cell (b)

circuit and a correspondent compression circuit are respectively shown.

The circuit in Fig. 4.a) is described by the following relation:

$$I_{out} = I_0 \exp\left(\frac{V_{diff}}{2V_T}\right) \tag{9}$$

$$\text{where } V_{diff} = V_+ - V_- \tag{10}$$

For the circuit in Fig. 4.b), the output voltage can be expressed in terms of the input current as:

$$V_{out} = 2V_T \ln\left(\frac{I_{in}}{I_0}\right) \tag{11}$$

For implementing the $\exp\left(V_{in}/(nV_T)\right)$ function, useful in the following application, the companding circuits in Fig. 5 are proposed. For the circuits in Fig. 5, $n-2$ linearization diodes for the branches, placed in the translinear loops have been used.

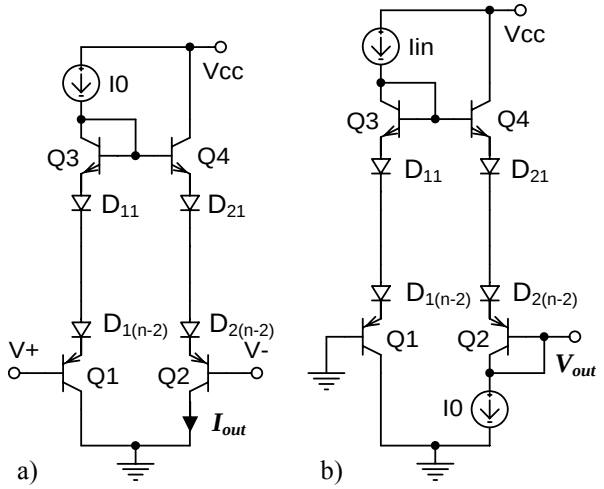

Fig. 5. Differential expanding cell (a) and correspondent compression cell (b) with linearization diodes

For the circuit in Fig. 5.a), the output current expression is:

$$I_{out} = I_0 \exp\left(\frac{V_{in}}{nV_T}\right) \tag{12}$$

and for the circuit in Fig. 5.b), the output voltage is:

$$V_{out} = nV_T \ln\left(\frac{I_{in}}{I_0}\right) \tag{13}$$

After calculation, the transconductance of the circuit in Fig. 5 can be expressed as:

$$G_m = \frac{dI_{out}}{dV_{in}} = \frac{I_0}{nV_T}\exp\left(\frac{V_{in}}{nV_T}\right) \tag{14}$$

Developing equation (14) in Taylor series, it can be approximated as:

$$G_{m0} = \frac{I_0}{nV_T} \tag{15}$$

As expected, by using the linearization diodes, the circuit's transconductance value has decreased n times (according to (15)), but the dynamic range of the input signal for which the circuit works linearly has considerably increased.

In Fig. 6 we show the circuit dc characteristic (output current vs. input voltage) for a variable number of linearization diodes.

The output current can be developed in Taylor series as follows:

$$I_{out}(V_{in}) = a_0 + a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 + \cdots \tag{16}$$

where:

$$a_0 = I_{out}(0) = I_0 \tag{17}$$

represents the dc component and

$$a_k = \frac{\delta^k I_{out}(0)}{\delta V_{in}^k}\frac{1}{k!}, \quad k = 1, 2, \ldots, n \tag{18}$$

is the magnitude of k order harmonic.

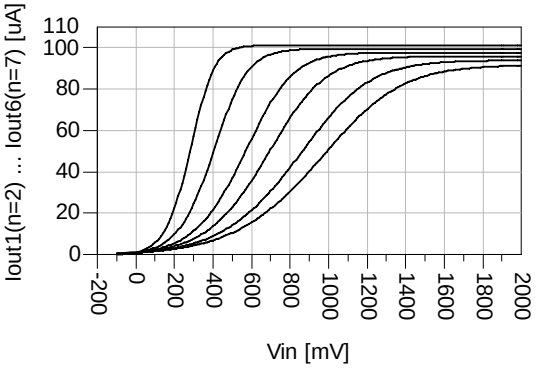

Fig. 6. The circuit's dc characteristic when the linearization diodes number is variable (n = **2, 3, 4, 5, 6, 7**); V_{cc} = **6V**; I_0 = **1µA**

Using (12) in (18) the following terms of Taylor series result:

$$a_1 = \frac{I_0}{nV_T};\quad a_2 = \frac{I_0}{2n^2V_T^2};\quad a_3 = \frac{I_0}{6n^3V_T^3} \tag{19}$$

3.1. The Linearity Error Calculation for the Proposed Differential Exponential Cell with Linearization Diodes

The linearity error can be expressed as:

$$\varepsilon = \left|\frac{I_{out\_lin} - I_{out}}{I_{out\_lin}}\right| \cdot 100 \ (\%) \tag{20}$$

where I_{out} is the output current and I_{out_lin} is the output current linearized expression, which can be approximated as:

$$I_{0\,lin} = I_0 + \frac{I_0}{nV_T}\cdot V_{in} \tag{21}$$

To make the calculation easier in (20), the output current I_{out} is considered as being formed of the first three terms of equation (16).

The dynamic range of the input signal for which the linearity error is $\varepsilon \le 1\%$ is:

$$V_{in}^{\varepsilon\le 1\%} \le \frac{a_1}{2a_2}\cdot\frac{1}{100}\left[1+\sqrt{1+400\frac{a_0a_2}{a_1^2}}\right] \tag{22}$$

Using (19) in (22), we obtain:

$$V_{in}^{\varepsilon\le 1\%} \le nV_T\left(\frac{1+\sqrt{201}}{100}\right) \tag{23}$$

In Fig. 7 the linearity error of the circuit in Fig. 5.a), when the linearization diodes number is variable is shown.

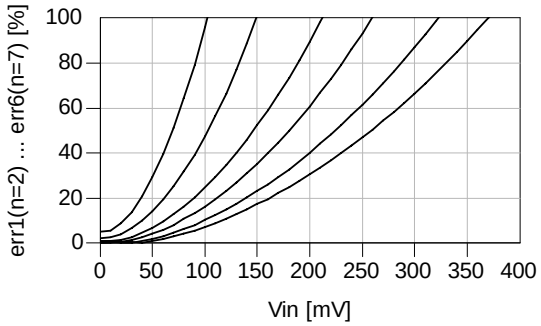

Fig. 7. The linearity error when the linearization diodes number is variable (n = **2, 3, 4, 5, 6, 7**); V_{cc} = **6V**; I_0 = **1µA**

3.2. *THD* Calculation for the Proposed Differential Exponential Cell with Linearization Diodes

The total harmonic distortion (***THD***) is calculated using the following equation:

$$THD = \sqrt{\sum_{n=2}^{\infty} HD_n^2} \tag{24}$$

where HD_k is the k order harmonic distortion. Considering the first two terms only, i.e.,

$$HD_2 = \frac{1}{2}\frac{a_2}{a_1}V_{in}; \quad HD_3 = \frac{1}{4}\frac{a_3}{a_1}V_{in}^2 \tag{25}$$

we obtain:

$$THD = \frac{V_{in}}{4nV_T}\sqrt{1+\frac{1}{36}\frac{V_{in}^2}{n^2V_T^2}} \tag{26}$$

The dynamic range of the input signal for which we have $THD \le 1\%$, is:

$$V_{in}^{THD\le 1\%} \le \sqrt{2}\frac{a_2}{a_3}\sqrt{-1+\sqrt{1+\frac{a_1^2a_3^2}{50^2a_2^4}}} \tag{27}$$

Using (19) in (27), we obtain:

$$V_{in}^{THD\le 1\%} \le nV_T\frac{\sqrt{6}}{5}\sqrt{\sqrt{5626}-75} \tag{28}$$

From (23) and (28) one can observe that the dynamic range of the input signal for which the circuit operates linearly increases simultaneously with the number of diodes placed in the input transistors' emitters, but at the price of a decreased value of circuit's transconductance, according to relation (15).
One can notice that all the relation above are also valid for circuit from Fig. 4.a) if we consider $n = 2$.

4. Implementing of Non-linear Mathematical Functions Using Log-domain Circuits

4.1. Divider

The divider circuit can be implemented by using the following mathematical relation:

$$\frac{I_1}{I_2} = \exp\left(\ln I_1 - \ln I_2\right) \tag{29}$$

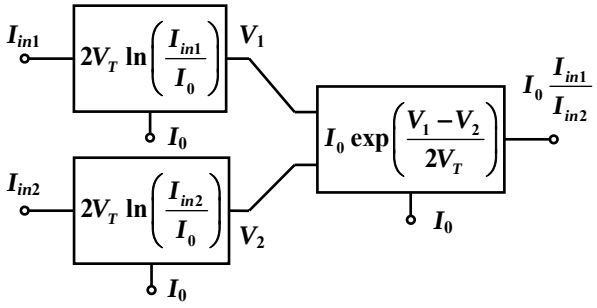

Fig. 8. The divider circuit principle

This function can be performed using the block schematic from Fig. 8.

In Fig. 9 the realization at a transistor's level of the block schematic from Fig. 8 is shown.

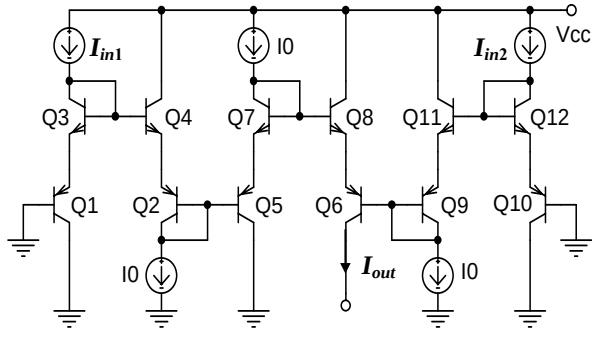

Fig. 9. Realization of the divider by log-domain circuits

4.2. N^{th} Order Rooter

The n^{th} order rooter can be implemented with the block schematic from Fig. 10.

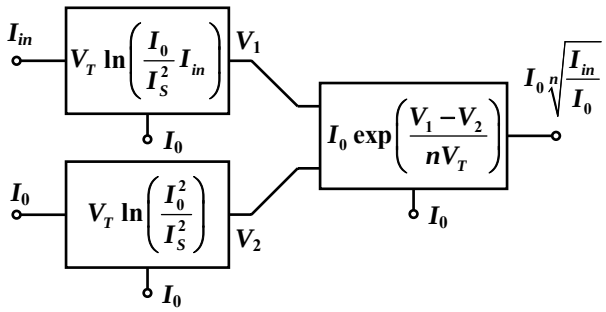

Fig. 10. The n^{th} order rooter principle

A transistor level realization of the block schematic from Fig. 10 is shown in Fig. 11.

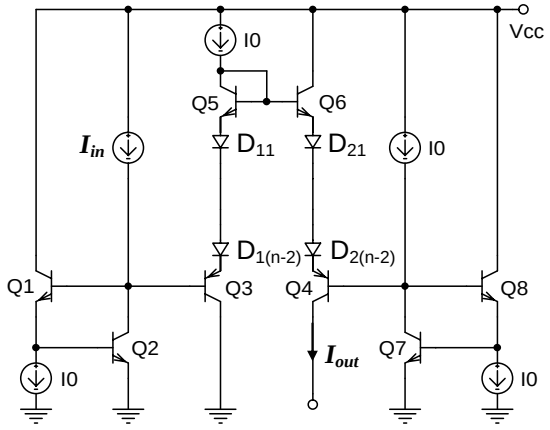

Fig. 11. Realization of the n^{th} order rooter using log-domain circuits

4.3. Exponentiation

An exponentiation circuit can be implemented with the block schematic presented in Fig. 12

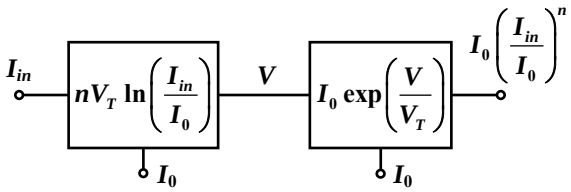

Fig. 12. The high-powers (exponentiation) principle

and in Fig. 13 the transistor level realization of block schematic from Fig. 12 is shown.

In all the realizations above, the I_0 bias current represents the scale factor.

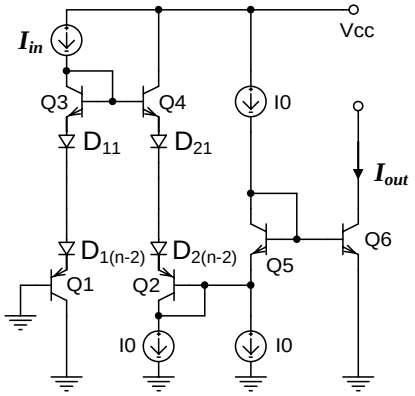

Fig. 13. Realization of the high-powers (exponentiation) using log-domain circuits

5. Simulation Results

In Fig. 14 the operation of the circuit from Fig. 9, which realizes the two currents division function is shown. In Fig. 14.a) the two input currents are presented: I_{in1} with constant value **0.7mA** and I_{in2}, triangular, having a **1MHz** frequency and **1mA** magnitude. In Fig. 14.b) is presented the resulting output signal, which is proportional to the ratio of the input signals (I_{in1}/I_{in2}). The scale factor is fixed by the bias current $I_0 = 1\mu A$.

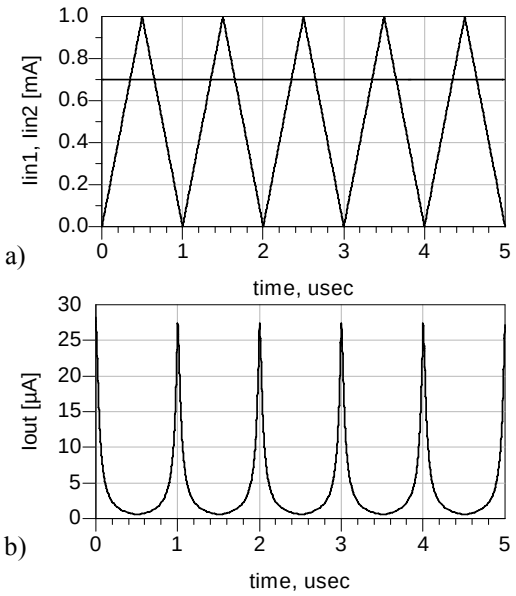

Fig. 14. The operation of the divider circuit: a) the input currents, I_{in1}=**0.7mA** and I_{in2}, having **T=1µs**; b) the ratio of the two input currents; V_{cc} = **3V**; I_0=**1µA**

In Fig. 15 is illustrated the operation of the **4**th order rooter circuit, according to the scheme shown in Fig. 11, where two linearization diodes for the branch were used. In Fig. 15.a) the triangular input current, with a **1MHz** frequency and **100µA** magnitude is presented. In Fig. 15.b) the output current, proportional to the **4**th order root of the input current, is represented.
The scale factor is fixed by the bias current $I_0 = 1\mu A$.

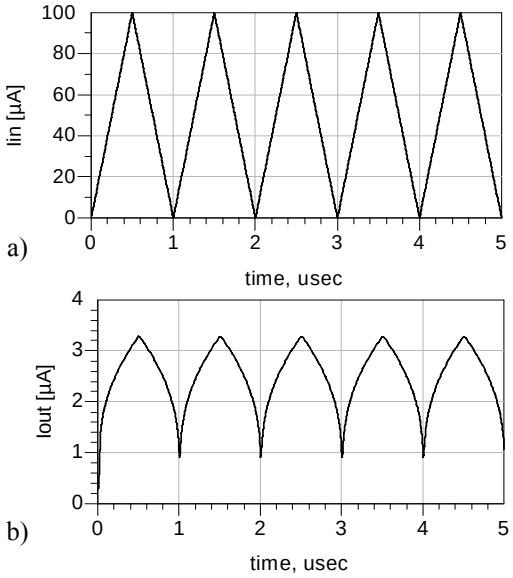

Fig. 15. The operation of the **4**th order rooter circuit:
a) the input current having **T=1µs**;
b) the **4**th order root of the input current;
V_{cc} = **4V**; I_0=**1µA**

In Fig. 16 the operation of the high-powers (exponentiation) circuit for $n = 4$, following the scheme from Fig. 13, in which two linearization diodes for the branch were used, is shown. In Fig. 16.a) we presented the triangular input current, with a **1MHz** frequency and a **2µA** magnitude and in Fig. 16.b) the output current, proportional to the raising to a power $n = 4$ of the input current, is shown.
The scale factor is established by the bias current $I_0 = 1\mu A$.

6. Concluding Remarks

In this paper several new methods for implementing non-linear mathematical functions using the log-domain circuits have been presented.
The methods consist of compensating the input and the output circuits' non-linearities, so that

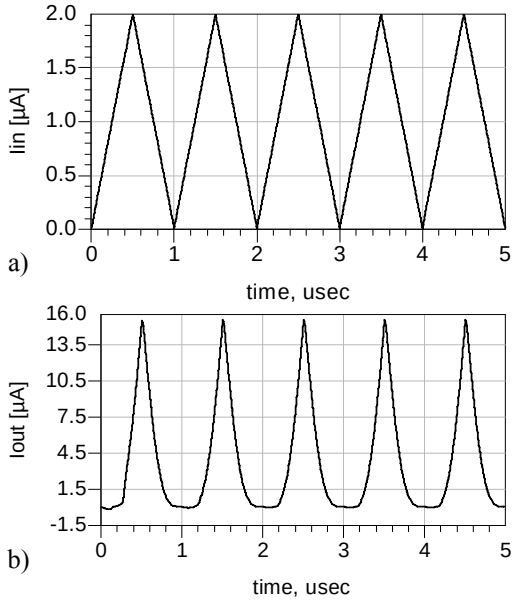

Fig. 16. The operation of the high-powers (exponentiation) circuit for ***n*=4**;
a) the input current having **T=1µs**;
b) the raising to a power ***n*=4** of the input current;
V_{cc} = **4V**; I_0=**1µA**

the resulted current mode circuit realize the desired mathematical function: division, n^{th} order root and raising to a power.
The obtained circuits are based on the logarithmic and exponential basic cells realized in 0.8 µm BiCMOS technology and are simple, easily to implement in silicon and have a good frequency response.
The 0.8 µm BiCMOS technology simulations confirm the theoretically obtained results.

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