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CONCEPTS OF ELABORATION AND ORGANIZATION OF COMPLEMENTARY RECONFIGURABLE ELEMENTARY DIGITAL STRUCTURES (CREDS) ON TWO LOGICAL LEVELS

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Abstract. *In this paper a method of elaboration of the CREDS on two logical levels is suggested. In [1] this problem is solved for circuits with three levels of logical gateways. The rapidity of data processing in two levels circuits is undisputable this is another argument for their elaboration. In [1] it was proposed to use the programmable logical modules (PLM) with a supplementary command input for amelioration of testability of designed digital circuits (DC). But there is no biunivocal correspondence among those four PLM structures proposed and respective Boolean functions (BF). They don't take in account all the synthesis process. The utilization example is artificial and non concludent using the MLP on three levels only. A reasonable objection could be the big apparatuses cots for (which actually is not a problem for the elementary circuits on crystals). But, when we speak about human lives and we need o make an extra fast testing of circuits, which will be made periodically and followed by a specific instructions using two tests only for the combinational circuits with a tens of primary inputs and hundreds or thousands of gateways, it doesn't make sense to refer to the costs. It is understood that also at this stage the circuit must be redesigned at the initial step for met a special goals, this could be the payment for assurance on easy testing of any combinational circuits using two tests only.*
Keywords: *synthesis, structure, reconfigurable, testability.*

Introduction

The traditional solution of the testing problem consists in reconsideration of the basics principles of the structure's synthesis respecting a series of restrictions concerning the use of a specific cost's degree with the scope to obtain more testable structures, which will permit to retrieve the spending at elaboration and start up of the tests. At the same time it is well known that modifying the circuit such as it will became more testable sometimes could arrive to the fact that the complexity of its synthesis and its production costs considerably increases. Unfortunately, there are no true statistics on the ratio of supporting the process of tests made and profit. The reason is as in the concurrence among the companies, which attends to establish their strong positions on the market as in the mercantile interests of some less known "schools" or, in general, the chase of money.

1. Aspects of the synthesis of the Complementary Reconfigurable Elementary Digital Structures on two logical levels

In order to make more convenient and comprehensible the following consideration of the problem of synthesis of the Complementary Reconfigurable Elementary Digital Structures (CREDS) on two logical levels we'll use the table of the complementary functions pairs with two informational inputs (table 1). In order to make the things simpler we'll consider for the first the pairs of the complementary gateways with two informational inputs: AND / OR, AND-NOT / OR-NOT, NOT-AND / NOT-OR, NOT-AND-NOT / NOT-OR-NOT. Before starting with describing the process of the synthesis of the complementary reconfigurable elementary digital structures we'll consider some particularities of the sinthesys of the combinational circuits in the operational basis different from simple Boolean operational basis AND, OR, NOT [2,3]. As shown in table 1, only the circuit, which corresponds to the $F_{1,2}$

structure can be present in simple Boolean basis. In general case the synthesis of the circuits of the complementary structures $F_{3,4}$, $F_{5,6}$ and $F_{7,8}$ can be made as: for the first the well elaborate procedure of the structure's synthesis in the simple Boolean basis further it is passed to the necessary sets of the logical gateways. Is not the same case with making synthesis of complementary reconfigurable elementary digital structures on two logical levels.

Table 1

Inputs		Complementary structures							
		$F_{1,2}$		$F_{3,4}$		$F_{5,6}$		$F_{7,8}$	
x	y	$F_1=xy$	$F_2=x\vee y$	$F_3=\overline{xy}$	$F_4=\overline{x\vee y}$	$F_5=\bar{x}\cdot\bar{y}$	$F_6=\bar{x}\vee\bar{y}$	$F_7=\overline{\mathbf{x}\cdot\mathbf{y}}$	$F_8=\overline{\mathbf{x}\vee\mathbf{y}}$
0	0	0	0	1	1	1	1	0	0
0	1	0	1	1	0	0	1	1	0
1	0	0	1	1	0	0	1	1	0
1	1	1	1	0	0	0	0	1	1

Table 1 (continued)

Inputs		Complementary structures							
		$F_{9,10}$		$F_{11,12}$		$F_{13,14}$		$F_{15,16}$	
x	y	$F_9=x\forall y$	$F_{10}=x\sim y$	$F_{11}=x\bar{\forall}y$	$F_{12}=x\overline{\forall}y$	$F_{13}=x\oplus y$	$F_{14}=x\bar{\oplus}y$	$F_{15}=x\bar{\oplus}y$	$F_{16}=x\overline{\oplus}y$
0	0	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	0	0	1
1	0	1	0	0	1	1	0	0	1
1	1	0	1	1	0	0	1	1	0

1.1. The particularities of the CREDS on two logical levels synthesis.

For the case the usual techniques of synthesis could not be used. The basic particularity of the CREDS' s synthesis on two logical levels consists in adding of a supplementary input for applying the command signal for each of the complementary gateways' pairs. This excludes the explicit indication of the basic gateway from the complementary gateways' pairs. That is, each of gateways from the complementary pair could be the basic one, but according to the algorithm, we'll choose only one gateway. The meaning of CREDS synthesis on two logical levels with two informational inputs (for three ore more inputs the procedure remain the same) and one command input consists in choosing such attributes of the logical values of the command signal C as they satisfy the necessary and sufficient condition of the CREDS' s functionality:

1) to the signal C will be assigned such a value as:

a) C will "activate" the "basic gateway" of the CREDS' s complementary pair, i.e. C will have the amazing value of the basic gateway' s signal;

b) C will "block" in CREDS the "complementary" gateway of the basic gateway, i.e. C will have the dominant value of the complementary gateway' s signal;

2) to the signal C will be assigned an opposed value to that described in point 1 such as:

a) C will "activate" in CREDS the complementary gateway of the pair, i.e. C will have the amazing value of the complementary gateway' s signal;

b) C will "block" the "basic gateway" of the CREDS, i.e. C will have the dominant value of the basic gateway' s signal;

These rules means that the attributes to the logical values of the command C signal will be assigned in a such a way in which the MODULO 2 SUM of the C' s signal and the value of the dominant C (blocking) signal of the gateway which should be deactivated will be cancelled.

For example, for the complementary pair $F_{1,2}$ the

basic gateway is AND, but the complementary one – the gateway OR.
For the C=1 should be activated the basic gateway AND and deactivated the complementary one OR:

$$\mathbf{F_{1,2} = (Cxy \oplus (C \vee x \vee y) \oplus C)\big|_{C=1} = (Cxy \oplus C \oplus C)\big|_{C=1} = xy} \ , \quad (1)$$

And vice versa, for the C=0 should be activated the complementary gateway OR and deactivated the basic one OR:

$$\mathbf{F_{1,2} = (Cxy \oplus (C \vee x \vee y) \oplus C)\big|_{C=0} = ((C \vee x \vee y) \oplus Cxy \oplus C)\big|_{C=0} = x \vee y} \ , \quad (2)$$

These intuitive and heuristic results we'll try to formalize in order to obtain a regular method of synthesis of the digital structures in the extents basis of Boolean operations. Such an approach it is not treated in the literature still.

2. Elaboration of the method of CREDS' s in two logical levels synthesis

In this case it is impossible to use the classical techniques of synthesis of the digital circuits and it is desirable to elaborate another method of the CD's synthesis.

2.1. $F_{1,2}$ CREDS' s synthesis

We'll effectuate the method's description for the case of the $F_{1,2}$ (tab. 1) CREDS considering that the basic gateway AND and the complementary gateway of this CREDS pairs – the OR one.
The process of CREDS synthesis suppose to follow these steps.
1^0. In the CREDS' s complementary pairs will be chosen the basic gateway. In this case it is AND gateway.
2^0. According to the (1), which describes the functionality of the $F_{1,}2$ CREDS in the logic of F_1 gateway – AND, we represent each component by using a separate Karnaugh map and making MODULO 2 SUM of the content of similar coordinates of those three maps, writing the result in the fourth Karnaugh map (fig. 1,a).
3^0. According to the (2), which describes the functionality of the $F_{1,}2$ CREDS in the logic of F_2 gateway – OR, we represent each component by using a separate Karnaugh map and making MODULO 2 SUM of the content of similar coordinates of those three maps, writing the result in the fourth Karnaugh map (fig. 1,b).
4^0. We effectuate modulo 2 summ between similar coordinates of the Karnaugh maps from the first two columns of the first row writing the result in the third column of the first row.
5^0. We effectuate modulo 2 summ between similar coordinates of the Karnaugh maps from the first two columns of the second row writing the result in the third column of the second row.
6^0. We effectuate modulo 2 summ between similar coordinates of the Karnaugh maps from the first two columns of the third row writing the result in the third column of the third row.
7^0. We effectuate modulo 2 summ between similar coordinates of the Karnaugh maps from the first two columns of the fourth row writing the result in the third column of the fourth row.
The verification of the correctitude of the result could be checked by making modulo 2 sum between similar coordinates of the Karnaugh maps from the first rows of the third column writing the result in the fourth row of the third column (fig. 1,c). The obtained result must be identical with that obtained from p.7^0.
8^0. According to the results from the Karnaugh map from the third column we build the table of the CREDS functionality ($F_{1,2}$ in this case - table 2).
9^0. According to the CREDS' s table of functionality we effectuate the synthesis of the respective structure (fig. 2).
The logical expression (3) describes $F_{1,2}$ CREDS' s general functionality and allows the implementation using a digital circuits with two logical levels. The possibility of CREDS' s synthesis on two logical levels allows the

increasing of data processing speed, a fact which is very important for the digital structures of the computers with an operative in real time data processing. The actual integrates' fabrication TTL technology allows the possibility to implement the MODULO 2 SUM gateway with the parameters approximately identical with those from AND-NOT one. [4].

Table 2. $F_{1,2}$ CREDS' s functionality table

x	y	C	$F_1=xy$	$F_2=x\vee y$	$F_{1,2}=F_1\oplus F_2\oplus C$
0	0	0	0	0	0
0	1			1	1
1	0			1	1
1	1			1	1
0	0	1	0	1	0
0	1		0		0
1	0		0		0
1	1		1		1

$$\mathbf{F_{1,2}=(F_1\oplus F_2\oplus C)|_{C=1}\oplus(F_2\oplus F_1\oplus C)|_{C=0}}$$

a) b) c)

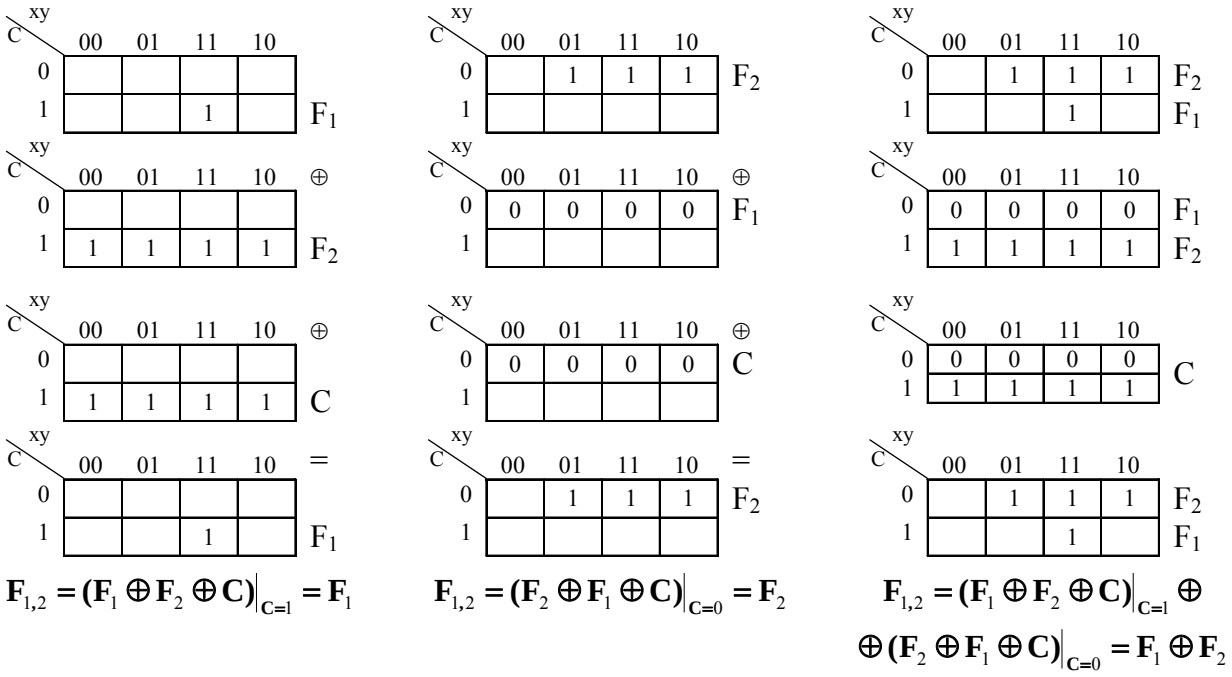
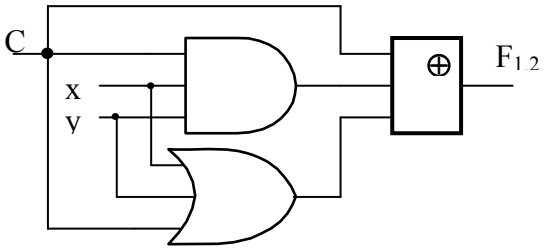


Fig.1. CREDS synthesis a) the functionality in the AND gateway logic; b) the functionality in the OR gateway logic; c) the functionality in the $F_{1,2}$ CREDS logic.



$$\mathbf{F_{1,2}=Cxy\oplus(C\vee x\vee y)\oplus C}, \qquad (3)$$

Fig. 2. CREDS $F_{1,2}$

Pay attention to the fact that logical expression (3) is invariant to those three its components, that's why, unlike to CREDS with three logical levels, which can have more realizations, CREDS which corresponds to the (3) expression can be implemented in only one way as shown in fig.2. Choosing the basic gateway for CREDS on three logical gateways' levels means that that gateway should have a supplementary command input C. Depending on which from the complementary gateways will be chosen like basic we'll get more variants of CREDS on three logical levels. The basic particularity of CREDS

on two logical levels consists in adding a supplementary input for the C signal for all gateways if complementary pair. These thesis (affirmations) are not available for CREDS on two logical levels synthesis.

3. The elaboration of the hyper testable structures using CREDS on two logical levels

The elaboration of the hyper testable structure could be made for the initial circuit represented in any basis – simple Boolean, mono functional, mixed or extended.

The concept of hyper testable circuits' elaboration in CREDS basis on two logical levels will be considered the following example.

Let's suppose that implemented logical function is:

$$F = \overline{abe \vee dgh}, \quad (4)$$

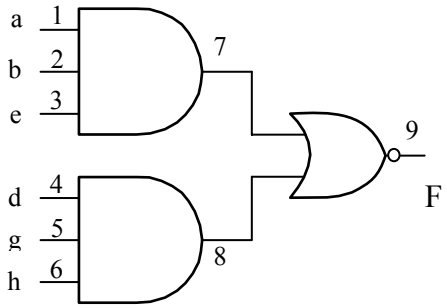


Fig. 3. Initial circuit

It is desirable to implement the following hyper testable structure.

From the initial circuit (fig.3) could be concluded that in the normal functionality state the gateways 7 and 8 should make the operation AND, but the gateway 9 - logical OR-NOT operation. The synthesis of the hyper testable structure consists in the following steps:

1^0. According to the remarked requirements we'll select $F_{1,2}$ type of CREDS for the first level' s gateways (surely with three informational inputs).

2^0. We'll select the $F_{3,4}$ type of CREDS for the second level' s gateway.

3^0. In the normal state of functionality according with relation (4) at the command inputs should be applied the signals C_1C_2=10. In this case will be activated the gateways 7_1, 8_1 and 9_1 and will be blocked 7_2, 8_2 and 9_2 (fig. 4,a).

4^0. In the first state of testing we'll choose the values for the command signals as circuit is changing into a maximal degenerate of AND type equivalent to the AND gateway with the same number of inputs. In only this case will be possible the detection of the ≡0 error at all circuit' s inputs by applying of an amazing set T_1= abedgh=111111. It is clear that we should select the 7_1, 8_1 and 9_2 gateways using for this case the set of the command signals C_1C_2=11 (fig.4,b). The presence of an inversor on the output connection doesn't affect the above stated concepts, the only one thing is that the output signal will be inversed.

5^0. In the second state of testing we'll choose the values for the command signals as circuit is changing into a maximal degenerate of OR type equivalent to the OR gateway with the same number of inputs. In only this case will be possible the detection of the ≡0 error at all circuit' s inputs by applying of an amazing set T_2= abedgh=000000. It is clear that we should select the 7_2, 8_2 and 9_1 gateways using for this case the set of the command signals C_1C_2=00 (fig.4,c). The presence of an inversor on the output connection doesn't affect the above stated concepts, the only one thing is that the output signal will be inversed.

It is clear that depending on selected values of the C_1C_2 command signals the circuit will work in the normal mode or in one of two testing' s states. This means that by applying of two sets of the logical values of the ipothetical complementary gateways' inputs signals could be detected ≡0, ≡1 errors of the inputs of initial circuit. So, in spite of numbers of inputs of the checked circuit and of number of gateways there will be necessary only two tests for complete testing of circuit, i.e. testing could be prevent like an included instruction in the functionality cycle of the computer or like an procedure made with an specified frequency which will stop the errors propagation. The possibility of hyper testing is great one for the computers specialized in real time processes command, where should be taken into account the human live - airplanes, aquatic Plaines, nuclear reactors or chemical one.

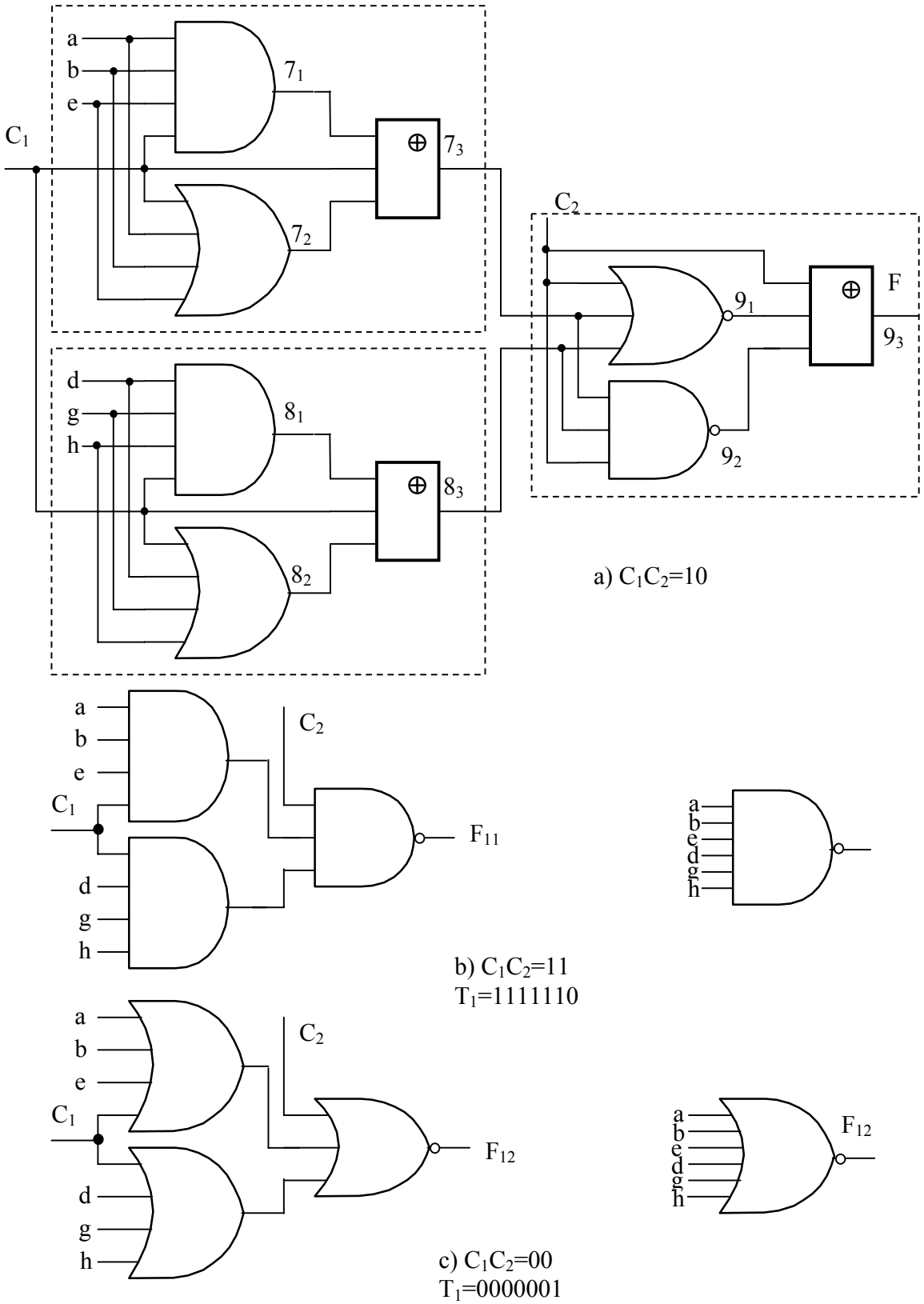


Fig. 4. The state of normal functionality (a), the first state of testing (b) and the second state of testing (c).

4. Conclusions

Analysing the Complementary Reconfigurable Elementary Digital Structures on two logical levels allows us to conclude:

1. CREDS on two levels of logical gateways allows a relative simple organization of the hyper testable circuits verified through an simple application of only two tests in spite of number of primary inputs and number of gateways.
2. CREDS on two logical levels allows an increasing of data processing.
3. The attribution of the logical values of the command signals will be made in such a way as cancelling MODULO 2 SUM of the C signal's value and C dominant (for blocking) signals' value of the deactivated gateway.
4. It was elaborated the synthesis method of CREDS on two logical levels in the MODULO 2 SUM basis, a fact which allowed to obtain a new qualitative results.
5. For the case when the complementary pair' s gateways contain inversors at the output the input into the MODULO 2 SUM gateway of the C command signal connection should also inversed for taking into a sin phase this value with the dominant C of the blocked gateway.
6. CREDS on XOR (EQUIVALENCE) gateways in the first level could be not implemented on two levels of logical gateways, but only in three levels.
7. CREDS on MODULO 2 SUM (PARITY) gateways in the first level could be not implemented on two levels of logical gateways, but only in three levels.
8. The synthesis of CREDS on gateways with more than three inputs is made in the similar mode.
9. Passing the minimal level of two informational inputs they produce an qualitative jump – the structure even reconfigurable (surely commendable) makes works like an only one function of only one variables - reapeater, or for the CREDSs inverting the gateways of the complementary pair, inversor. The meaning of this effect shoul be additional studied and it will be given an explanation for this phenomenon.

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