7th International Conference on DEVELOPMENT AND APPLICATION SYSTEMS
Suceava, Romania, May 27 – 29, 2004

ANALYSE OF PASSIVE METHODS TO INCREASE TESTABILITY OF DIGITAL STRUCTURES

Ion COJOCARU
"Politehnica" University of Bucharest
Splaiul Independentei 313, RO-7206 Bucharest
i_coj@yahoo.fr

Abstract. *Definition of testability design means the totality of measurement and condition of digital structures (DS) elaboration what contributes to minimise the cost of verification of correct works.*
Is analysed divers method of increase of controllability and observability. Estimate the parameters what's characterised the testability and estimate cost to obtain DS with increased testability. Obvious the advantage and shortcoming passive resource to increase testability of DS and is propose the solution to increase of DS testability compare the obtained result with results obtained with known method.
Key words: *Controllability, observability, testability, elaboration, structure, digital.*

Introduction

The growth in the number of active components placed on a chip up to several million and even tens million has had beneficial consequences such as the decrease in cost by a number of orders and the improvements of parameters. But the old "heritage" still persists which is the problem of the determination of good functioning of a chip at a reasonable price. This testing problem includes two principal aspects [1,8] – the generation of tests and the verification of tests. The generation of tests presumes the determination of a set of stimulating vectors, the application of which at the circuit inputs allows us to obtain the respective current reactions at the output, the coincidence of which with the model reactions, established a priori, would indicate the absence of certain defects. The verification of tests consists in demonstrating the fact that the set of tests effectively confirms the proper functioning of the circuit. At present, formal demonstrations of this fact are unknown, and the modelling of errors remains the only possibility which allows for a quantitative estimation of the tests efficiency. The performance of the synthesis of test sets by automate systems and by systems of errors modelling based on such tests declines drastically, while some manufacturers reject strict methods of verification, taking risks of producing deficient circuits. The solving of this problem may be achieved using an integral arsenal method known as "design for testability".

The key phase "testing design" comprises two sets of ideas which are in the permanent interaction and thus generate the concept of the idea of the design and diagnostics integration. The notion of design for testability covers all the measures and conditions for the realisation of a digital structure, which would contribute to the reduction of expenses inherent in the verification of accuracy of its functioning. Surveys on this problem as well as multiple variants of its solution are mentioned in [1, 8].

1. Passive means of maintenance

The suggestions regarding the increase of testability should be formulated at the level of the circuit structure as well as at the system logical level. The measures for testability maintenance at the structure level can be implemented within the computer aided automated design. Due to the above, we will focus on the establishment of measures meant to increase the testability at the system logical level.

In this work is proposed the passive resource to increase testability of combinational circuits

(CC), in base to assure possibility to reconfigure from normal mode of working in control regime. In this scope is useful hardware redundancies in sense to utilise in same way an additional chip and additional input contact. This concept conducts to obtain extratestability CC, verification of correct work that can be effectuate just with two tests. For sequential circuits (SC) is proposed to specific organise of trigger and synchrony sequential structures, what permit to effectuate it extratestability with four tests.

2. Primitives and definitions

In order to increase the comprehensibility of explanation of the considerated problem, we'll precise the basic notions and definitions of approach at the necessary level to the synthesis of the complementary circuits on 2 levels. According with the tables below of the logical gateways it is possible to mention two types of relations:

a) between the input and output signals of the same gateway;
b) between the input and output of the signals of two different gateways.

In other words, we'll establish several gateways' features studying the liaison between the logical values of the input signals and output, further we'll establish several features and relations between some couples of gateways. In the same way, the logical signal «0» applied at only one input of AND, AND-NOT gateway determines univocal the respective logical signal at the output.

The logical dominant value (for blocking) of the logical signal of the gateway's input means the logical value of the signal, which being applied at only one input, defines the binary signal of the gateway's output. For example, the logical signal «1» applied at only one input of the OR, OR-NOT gateways defines univocal the corresponding logic signal at the gateway's output. In the same way, the similar logical signal «0» applied at only one input of the AND, AND-NOT gateways defines univocal the corresponding logic signal at the gateway's output.

The amazing logical value of the gateway's input's signal means the logical value of the signal, which being applied concomitant at the all inputs defines the logical signal at the gateway's output. The set of the amazing logical values of all gateway's inputs' signals is called the amazing set. In other words, the set of the inputs' signals to which corresponds the unique logical value opposed to all the gateway's outputs' signals is called the amazing set. The meaning of the amazing set consists in the capacity of all respective gateway's inputs' errors $\equiv 0$ ($\equiv 1$) detection by using a single stimulus vector.

It is important to mention the following proprieties:

1. The logical values dominant and amazing of the NOT-AND (NOT-OR) gateway's inputs are opposed to the respective values of the AND (OR) gateway;
2. The specific of having dominant and amazing value of the signal it is common for the gateways with at least 2 inputs. So, the repeater and invertor can't have the dominant and amazing value of the signal. This is clear also from the fact that inversion and repeating are unitary operation, it means that they process only one operand ;
3. The gateways with 2 inputs XOR ($\forall$) and EQUIVALENCE ($\sim$) and the gateways with three and more inputs – MODULO 2 SUM and PARITY ($\overline{\oplus}$) don't have dominant and amazing values of the inputs' signals;
4. Fixing a signal for one input of the XOR (EQUIVALENCE) gateway in «0» («1») leads to the repeat (inversion) function execution of the signal of an other XOR gateway's input or to the inversion (repeat) function execution of the signal of an other EQUIVALENCE gateway's input.

There are specific relations among the gateways' features. Only those gateways will be equivalent which true tables are the same. For example, the following gateways are equivalent AND/NOT-OR-NOT, OR/NOT-AND-NOT, NOT-AND/OR-NOT, NOT-OR/AND-NOT. The meaning of the equivalent gateways consists in fact that at the replacing of one gateway with an

other equivalent, the functionality of the resultant circuit doesn't change.
We will call two gateways with the same number of input dual, if for each set of the values of the input signals the logical values of the output signals of the gateways are mutual opposed. For example, the following couples of gateways are called dual AND/NOT-OR, OR/ NOT-AND, AND-NOT/NOT-OR-NOT, OR-NOT/NOT-AND-NOT, XOR/EQUIVALENCE (only for two variables), MODULO 2 SUM/ PARITY. It is easy to understand that adding or omitting of an inversor at the output of the couple of gateways will change the relations' status among these gateways, passing form the equivalence to the duality and vice-versa. The meaning of the duality notion consists in using of the dual reconfigurable elementary structures in the synthesis of the hyper stable digital circuits, but for the permanent testable digital structures, which are tolerant to the errors – using duals one.
The set of which values of the binary signals are the same is called homogeny. For example, homogeny are the sets of the binary signals as 00, 11, no homogeny are the sets as 01, 10.
We will call complementary two gateways which have the same number of inputs, if applying of any no homogeny sets inputs binary signals, the gateway's outputs' signals are opposed. For example, the complementary gateways are AND / OR, AND-NOT/OR-NOT, NOT-AND/NOT-OR, NOT-AND-NOT/NOT-OR-NOT, XOR/EQUIVALENCE, MODULO 2 SUM/ PARUTY.
The meaning of the elementary complementary reconfigurable structures consists in having the possibility to se them like the most important component of the elaboration concept of the hyper testable combinational circuits. On other hand, the complementary combinational circuits are the basis of the concepts of elaboration of the digital structure permanent testable and errors tolerant.

3. Develop concept analyse and organise the testable combined circuits

Developing and organise of testable combined circuits means to increase the number of input and output pins, choose the method of syntheses and a base of logical operations, what is increased the complexity of circuit develop. This is the cost of simplification of testing procedures.
Reddy [7] has defined an easily testable network as one having the following properties: (1) small test set; (2) contains no logical redundancy; (3) structure of the test set is such that it is both easy to generate and integrated the results; (4) faults locatable to the desired degree; (5) test set can be derived without much extra work, either during the design phase or after the network is defined.
This list is qualitative only, but for the purpose of this paper it will serve as a working definition for "easily testable" circuits. Various other properties [1] may also be desirable and can be added to the list: (6) final gate-count should non be excessively high compared with a "normal" implementation; (7) minimum number of additional primary control inputs and observable output used to enhance testability.

3.1. Method Reddy

Theoretical base to choose logical circuits base to realise the function $F(x_1, x_2, \ldots, x_n)$ [7] is represented in form of decomposition Read-Muller (Read – Muller Expansion Technique).

Boolean function (FB)

$$F(x_1, x_2, x_3) = x_1 x_2 \vee \bar{x}_1 x_3 \vee \bar{x}_2 \bar{x}_3 \qquad (1)$$

It may be represent in Readdy-Muller discompose in this mode:

$$F(x_1, x_2, x_3) = 1 \oplus x_2 \oplus x_1 x_2 \oplus x_1 x_3 \oplus x_2 x_3 \qquad (2)$$

Logical scheme of representation FB (2) is showing in fig. 1, they verifying tests is: [7].
Conclusion: Succession structure of tests doesn't depend by number of variable and contain only four tests plus two necessary verifications tests of AND gates.
In this work [7] was demonstrated that detection all single errors $\equiv 0$, $\equiv 1$of one consecutive circuits by XOR gates need to apply on each entering gates XOR a trivial tests, structure of succession stimuli vectors that don't depend number of variables and contain only four tests.

Without this needs a stimuli vectors for verifying AND gates [10]. Reunion this two multitudes allowed obtain test:

$$T=n+4, \quad (4)$$

Disadvantaging of this method is growing complexity of realisation circuits and a number of logic levels, which influence technical characteristics [10].

Z	x_1	x_2	x_3
0	0	0	0
0	1	1	1
1	0	0	0
1	1	1	1

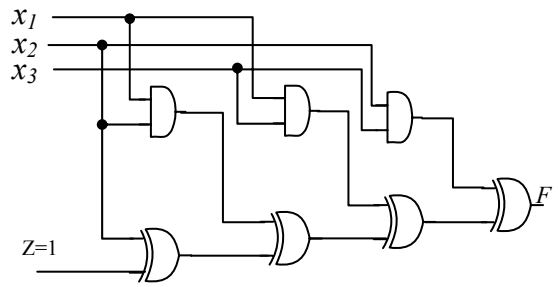


Fig. 1 Realization FB $F(x_1,x_2,x_3)=x_1x_2 \vee \bar{x}_1x_3 \vee \bar{x}_2\bar{x}_3$ reprezented in discompouse Readdy-Muller form

3.2. Method Readdy - Dandapani

One of method that allow reduction number of levels is elaborating structures OR-AND-OR [4] testable CC on three logical levels. The main trouble at these methods is strict limitation of type realisation function.

3.3. Method Hayes

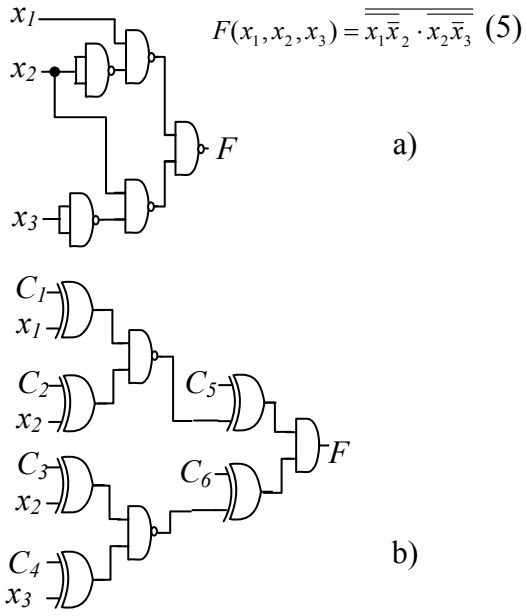
Testability of CC depends in direct mode by controllability (C) and observability (O). These characteristics may be ameliorate by introduce supplementary gates in scope growing number of entrees and out. These technique premise to modify CC and obtain sets that contain only five tests, that allow detection all errors CC [3]. The synthesising process once CC propose:

1°. FB is achieve in base 2NAND, NOT

2°. Each inverter is substituting with gate XOR, there one input is fixed in "1".

3°. Other input of the gates 2NOT-AND same include gates XOR one input of their is fixed in "0", this inputs been supplementary. Using these technical will considerate for FB [9,10] that realisation in base 2NOT-AND is showing in fig. 2, *a*

Proceeding succeeding generation of tests consist from obtain input succeeding, corresponding quotation multitude. After that is determine succeeding of inputs for supplementary input of CC (gates XOR) in this mode, on inputs corresponding gates 2NOT-AND to form same succession that there application result on inputs of gates, 2NOT-AND to be succession that belong these multitude. Using proceeding for CC from fig 2, b obtain succession from 5 test (fig. 2, c) [4].



$$F(x_1,x_2,x_3)=\overline{\overline{x_1\bar{x}_2}\cdot\overline{x_2\bar{x}_3}} \quad (5)$$

x_1	x_2	x_3	C_1	C_2	C_3	C_4	C_5	C_6
0	1	1	1	0	0	1	1	0
1	1	0	0	1	1	0	0	0
1	0	1	1	1	1	0	0	1
1	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	1	1

c)

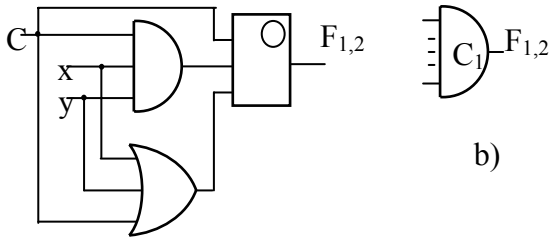
Fig. 2. Realization function $F(x_1,x_2,x_3)=x_1\bar{x}_2 \vee x_2\bar{x}_3$ in base 2 NOT/AND (a) their modification with XOR gates substation and include gates XOR on other inputs. (b) Succession verification tests (c)

4. Concepts of elaborating CC extratestable in base of elementary reconfigurable of digital structures

The utilization of reconfiguration for the purpose of improving the testability of CC was proposed in [3]. One of the ways of the organization of extratestable structures is connected with the elaboration of elementary reconfigurable digital structures (ERDS), of an elementary circuit for changing parity (ECCP) of binary signal.

In [3] dual ERDS (DERDS) were proposed, in [3] complementary ERDS (CERDS) were proposed, in [3] proposed were the concepts of the organization of extratestable CC.

Two logical parts with the same number of inputs are called dual if the signals at their outputs are reciprocally opposite for every combination of input signals. For instance, CERDS of $F_{1,2}$ AND/OR is shown in fig. 3, its functioning being described by boolean function (b) and table 1.



b)

$$F_{1,2} = Cxy \oplus (C \vee x \vee y) \oplus C$$

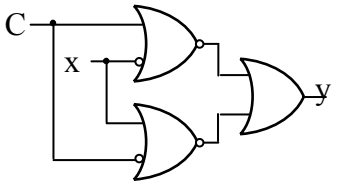
a)

Fig.3. CERDS of $F_{1,2}$ (a) and the symbol of representation (b)

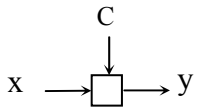
Table of function CERDS Table 1

x	y	C	F_1=xy	F_2=x∨y	$F_{1,2}$=F1⊕F2⊕C
0	0	0	0	0	0
0	1			1	1
1	0			1	1
1	1			1	1
0	0	1	0	1	0
0	1		0		0
1	0		0		0
1	1		1		1

An elementary circuit for changing parity (ECCP) [6] and the symbol of its representation are shown in fig. 4. its functioning being described by FB (7) and table 2.



a)



$$y = C\bar{x} \vee \bar{C}x \text{ , (7)}$$

b)

Fig.4. ECCP (a) and the symbol of representation (b)

Tabel 2. Tabel of function ECCP

C	x	a	b	y
0	0	0	0	Repeat x
0	1	1	0	
1	0	0	1	Inverse x
1	1	0	0	

Concepts of elaborating extratestable structures will consider in base FB described by expression (5) and contain next steps.

1º. Analyzing expression (5) rendering that she contain only gates AND, OR (fig. 5., a)

$$F = x_1\bar{x}_2 \vee x_2\bar{x}_3, \quad (8)$$

2º. Select from multitude CERDS structure $F_{1,2}$=AND/OR, for gates from other logical levels.

3º. Synthesize circuit with CERDS (fig. 5, b).

4º. Analyzing the present counter-claim fan-out with different parity of signals. One these input is input x_2. For assured change input x_2 parity in testable form we place one ECCP after inverter, signal c=0 that don't influence input signal x_2 (in normal ruining process), but c=1 in testable form invert supplementary signal on output, inverter on connection x_2.

5º. In normal function form on commands inputs $C_1C_2 = 10$, that conduced on activate gates 4_1, 5_1 and 6_1.

6º. In testable function "1" $C_1C_2 = 11$ fig. 5. c, that conduced on reconfigured structures in to maximal degenerate circuit of type AND, equivalent with gate AND with same number of inputs. Verifications all errors ≡0 of inputs gate AND it make with only one test - 111…1, inverting only inputs where stand the inverter.

7º. In testable function "2" $C_1C_2 = 00$ fig. 5. d, that conduced on reconfigured structures in to maximal degenerate circuit of type OR, , equivalent with gate OR with same number of inputs. Verifications all errors ≡1 of inputs gate OR it make with only one test - 000…0, inverting only inputs where stand the inverter.

Then, indifferent number inputs of gates, number and type of gates, to present fan-outs with diverse gates for testing the CC two tests are sufficient.

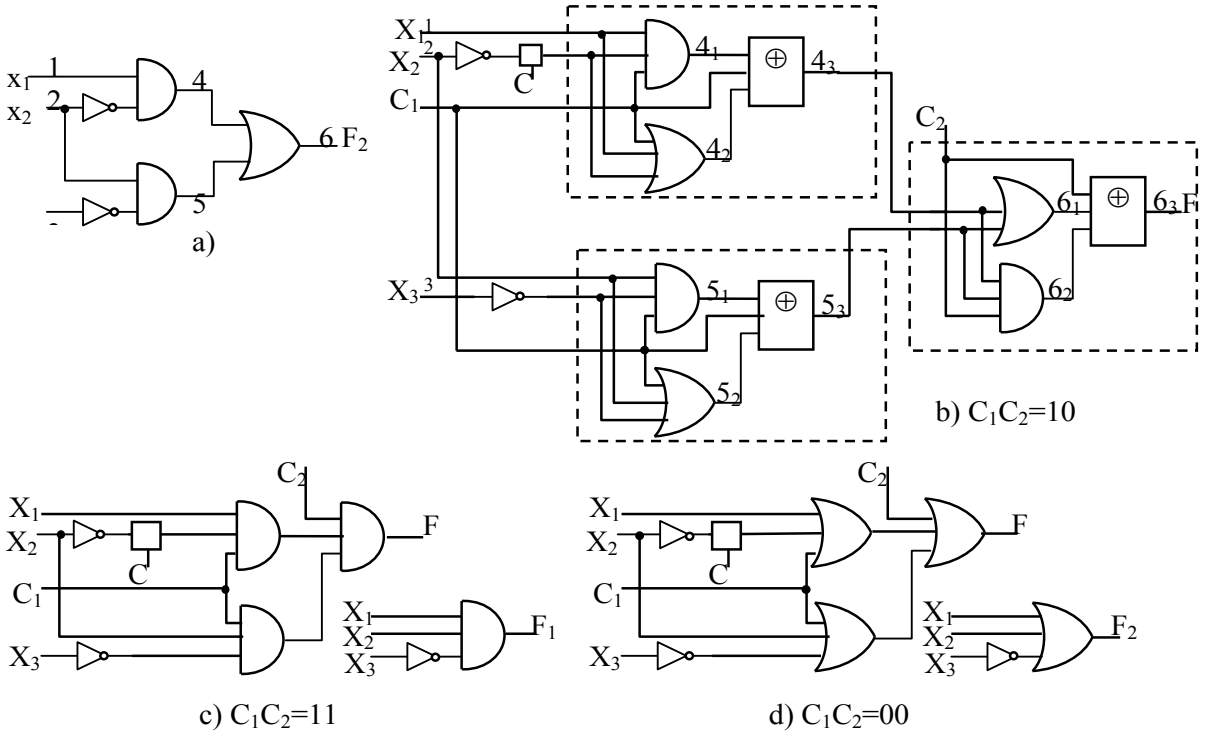


Fig 5. Initial circuit (a), normal function form (b), test regime 1 (c), test regime 2 (d).

Such concepts for development of extratestable structures are valid also for the arbitrary circuits with reconvergent fun-outs with different parities and initially synthesized in any basis of Boolean operators.

5. The analysis of the passive possibilities for the testability improving of the sequential circuits.

The proposals concerning testability improving must be formulated at the logical circuit's, device's and system's level. The accepted measures for the testability's guarantee at the structure's level can be achieved through the designing with computer assistance, for this reason, it's important to consider some aspects of the passive possibilities for growth T at the logic's level and the system's level [9]. The problems which are bound with the testability's guarantee of the sequential circuits (SC) are determined by a feature of SC working: the presence of the triggers requires the guarantee as for their installation at least in one of an initial state and for identification of the current state.

5.1. The partition of the tested system

This principle is used as the complexity of the problem of generation tests grows proportionally

to the third degree of the number of gates. A simple partition can be achieved by using the circuit's architecture with bus, which ensures the access to the checked sides of the system, by using the respective command logic. The architecture with bus partitions the plate so that all modules can be tested. Disadvantage of the systems with structured bus is associated with the bus's defects because such defect can be attributed to any module or to the bus.

5.2. Testable structured design

The easiest method of the SC modification is its division in two component parts – combinational and sequential by independent later checking one from another.

5.3. The scanpath method

This method reduces the SC testing to the CC testing. The scanpath's idea appears from the necessity to scan the input/output circuits used, in 1964, by IBM in SYSTEM/360. But in those circuits the entry and the reading of datas in register was made through the datas path. This is the difference between this method and scanpath method. Use of the triggers for the made of scanpath was done for the first in the diagnosis system NEAC – 2200/700, appeared in 1971.
In 1973 Williams and Angell have communicated about the scanpath's circuit orientated to an shifter. Toth and Holt from firma "Xerox" have communicated about scanpath's circuits which used an universal integral microcircuit of the shifter.

5.4. Random Access Scan

The random access scan (RAS) method's principle consist in possibility to address each memory element (ME) of the circuit for the installation, reset or observation its state independent from the others ME.

5.5. Level Sensitive Scan Design – LSSD

LSSD is the structured method for design of the testable structures elaborated by firma IBM. The method has two peculiarities:

1. the circuit's states can be changed only in accordance with design signal's level and not its front;
2. the circuits has guaranteed the property of the scanpath by latch triggers in two levels.

References

[1] Bennetts R., Scott R. (1976) *Recent developments in the theory and practice of testable logic design,* Radio and Electronic Engineer, vol. 45, No. 11, pp 667-679.

[2] Chang Chin Sheng, Oh Se Jeung (1975) *Testability enhancement in digital system design,* New York, IEEE Intercon. Conf. Rec. 11.3/1-7.

[3] Cojocaru Ion (2004) *Concepte de elaborare a structurilor extratestabile,* in curs de apariție.

[4] Dandapani R., Readdy S. (1974) *Other design of logic networks with rendundancy and testability considerations,* IEEE Trans. Computers, C-23, pp 1138-1149.

[5] Hayes J. (1974) *On modifying logic networks to improve their diagnosability,* IEEE Trans. Computers, C-23, No. 1, pp 56-62.

[6] Lala P. (1985) *Fault tolerant and fault testable,* London, Hardware design.

[7] Reddy S. (1972) *Easily testable realisation for logic functions,* IEEE Trans. Computers, C-21, No. 11, pp 1183-1188.

[8] Williams T. W., Parker K. P. (1982) *Design for testability,* A survey// IEEE Trans. Comput., 1982, N.1, p. 2-15.

[9] Zerbst M. (1986) *MEB-UND PRUFTECHNIK,* Berlin, Heidelberg, Springer-Verlag.

[10] Ярмолик В. (1988) *Контроль и иагностика ЭВМ,* Минс