

SEVERAL TIMING PARAMETERS FOR MULTIFUNCTIONAL DIGITAL CIRCUITS

¹ Alexandru VALACHI

² Mihai TIMIȘ

Technical University “Gh.Asachi” Iasi
Automatic Control and Computer Science Faculty
Computer Science & Engineering Department

¹ avalachi@cs.tuiasi.ro

² mtimis@cs.tuiasi.ro

Abstract. In this paper we present a new method for estimate of the timing recovery – t_{rec} , time removal – t_{rem} for the digital logic structures with memories and asynchronous mode inputs. Is prove that isn't necessary to implement the free hazard digital structure, but in this case it need a carefully analysis of the time recovery – t_{rec} . Usually, time removal – t_{rem} can be considered null, because from the calculations it has the negative value.

Keywords: Finite State Machine, Time recovery, Time removal, TTL circuits, CMOS circuits, Medium Scale Integration, Lower Scale Integration.

1. Introduction

Like in [1], implementation of finite automata is quite easy to do if we use multifunctional sequential circuits, figure 1.

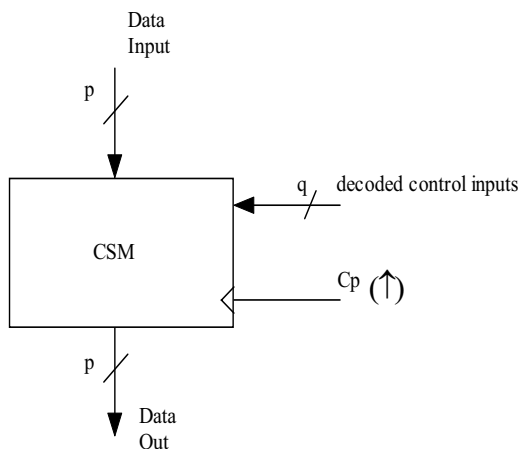


Figure 1. Finite automata.

We will consider the next timing values:

- t_{rec} – control mode setting up time ($t_{recovery}$)
- t_{rem} – control mode removal time ($t_{removal}$)

These times has the same semnification such as:

- $t_{s-u}(D)$ – time set-up data from clock's command front;
- $t_h(D)$ – time hold data from the same clock front;

Logic circuits timing parameters discussion is showing in [2]. In [3] is showing the timing

parameters for $t_{s-u}(D)$, $t_h(D)$, T (clock period), f (frequency clock).

In some databooks, t_{rec} , t_{rem} are associated with t_{s-u} , t_h , they must be mentioned separated. In this paper we propose a procedure for estimate it.

Lets consider the digital device showing in figure 2.a, with functional table such as in figure 2.b.

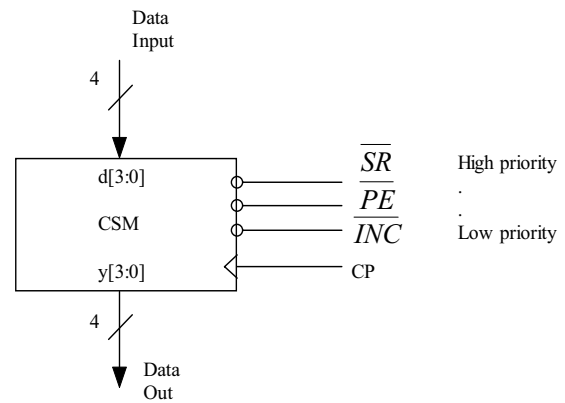


Figure 2.a. Finite automata.

| Mode | \overline{SR} CP | \overline{PE} ↑ | \overline{INC} 0 | $y[3:0]_{n+1}$ | Descriptor |
|-----------|-----------------------|----------------------|-----------------------|-------------------|------------------------|
| Hold | 1 1 | 1 X | | $y[3:0]_n$ | - |
| Reset | 0 X | X ↑ | | 0000 | - |
| P. Load | 1 X | 0 ↑ | | $d[3:0]_n$ | Paralell load Register |
| Increment | 1 | 1 ↑ | 0 | $(y_n+1)_{mod16}$ | Binary counter |

Figure 2.b. Functional table.

The digital circuit from figure 2.a can be implemented like in figure 3.

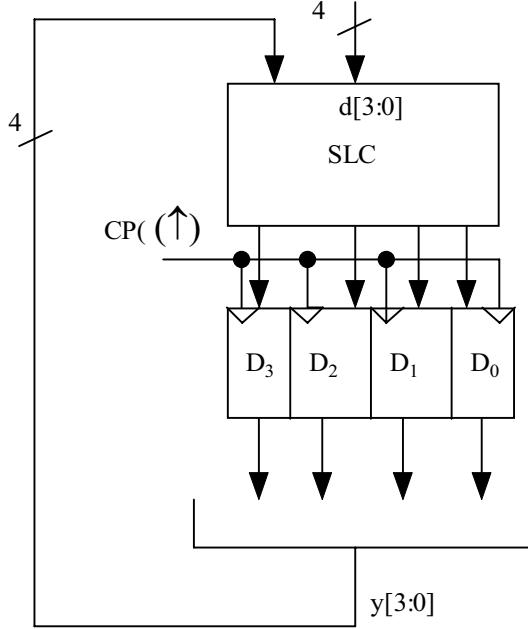


Figure 3. Implementation.

Using the functional table from figure 2.b, we can write equations for the D_j input signals:

$$D_j = \overline{SR}[PE \cdot d_j + \overline{PE}(INC \cdot \varphi_j + \overline{INC} \cdot y_j)] \quad (1)$$

$$\varphi_0 = \overline{y_0}; \varphi_1 = y_1 \oplus y_0; \varphi_2 = y_2 \oplus (y_1 y_0);$$

$$\varphi_3 = y_3 \oplus (y_2 y_1 y_0)$$

Binary counter implemented with CBB D circuits.

Mode inputs notated with $\overline{SR}, \overline{PE}, \overline{INC}$ are asynchronous relatively with the CP clock, and they have the priority such as in figure 2.a.

2. Calculation of the t_{rec}, t_{rem} parameters

If the circuit is on HOLD state, the functional mode change is accepted if the correspondent input is activated on a minimum time before the clock front CP.

In figure 4.a is showing the RESET command timing diagram.

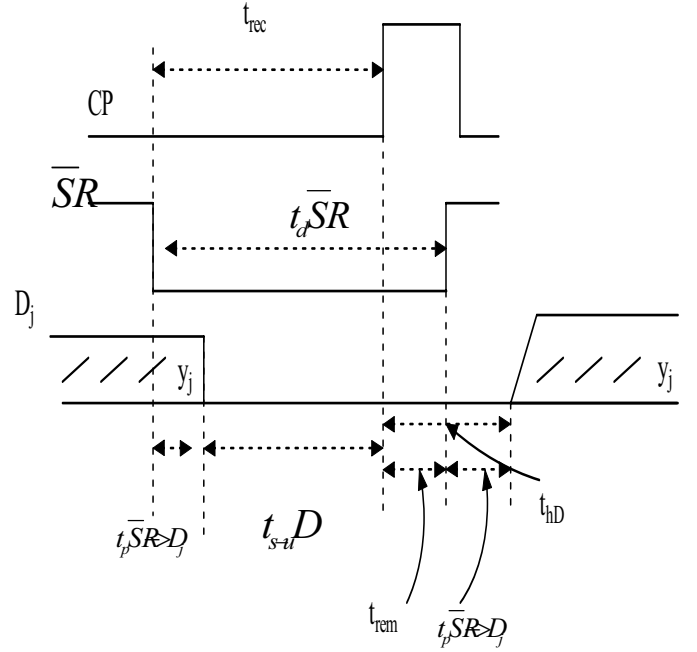


Figure 4.a. Timing analysis.

It can be observed that in the respective case, the $t_{s-u}(D), t_h(D)$ catalog variables must be respected according with CBB D implementation.

From figure 4.a we have (2) equation:

$$\begin{aligned} t_{rec}(\overline{SR}) &= t_{s-u}(D) + t_p(\overline{SR} \rightarrow D_j) \\ t_{rem}(\overline{SR}) &= t_h(D) - t_p(\overline{SR} \rightarrow D_j) \end{aligned} \quad (2)$$

Obs.

The $\underline{x}, \overline{x}$ variables are represented the minimum and maximum of x.

From (2) equation, can be estimated that t_{rem} can have negative values, usually set $t_{rem} = 0$.

The minimum duration of the \overline{SR} signal is:

$$t_{d}(\overline{SR}) = t_{rec} + t_{rem} = t_{s-u}(D) + t_h(D) + t_p(\overline{SR} \rightarrow D_j) - t_p(\overline{SR} \rightarrow D_j) \quad (3)$$

Usually $t_p(\overline{SR} \rightarrow D_j)$ isn't indicated in

databooks, so as to can be considered in the next equations:

$$\underline{t_p(\overline{SR} \rightarrow D_j)} = \frac{1}{2} \overline{t_p(\overline{SR} \rightarrow D_j)} \quad (4)$$

$$\underline{t_d(\overline{SR})} = \underline{t_{s-u}(D)} + \underline{t_h(D)} + \frac{1}{2} \overline{t_p(\overline{SR} \rightarrow D_j)} \quad (5)$$

The other parameters, $\overline{PE}, \overline{INC}$ are calculated using the above algorithm. Finally, we can write:

$$\underline{t_{rec}(CSM)} = \underline{MAX}[t_{rec}(\overline{SR}), t_{rec}(\overline{PE}), t_{rec}(\overline{INC})]$$

$$\underline{t_{rem}(CSM)} = \underline{MAX}[t_{rem}(\overline{SR}), t_{rem}(\overline{PE}), t_{rem}(\overline{INC})] \quad (6)$$

In calculation of the t_{rec}, t_{rem} timing, was not considered the hazard generated from the combinational logic structure.

3. Static hazard considerations

In figure 4 is presented a possible implementation for D_j , according with equation (1).

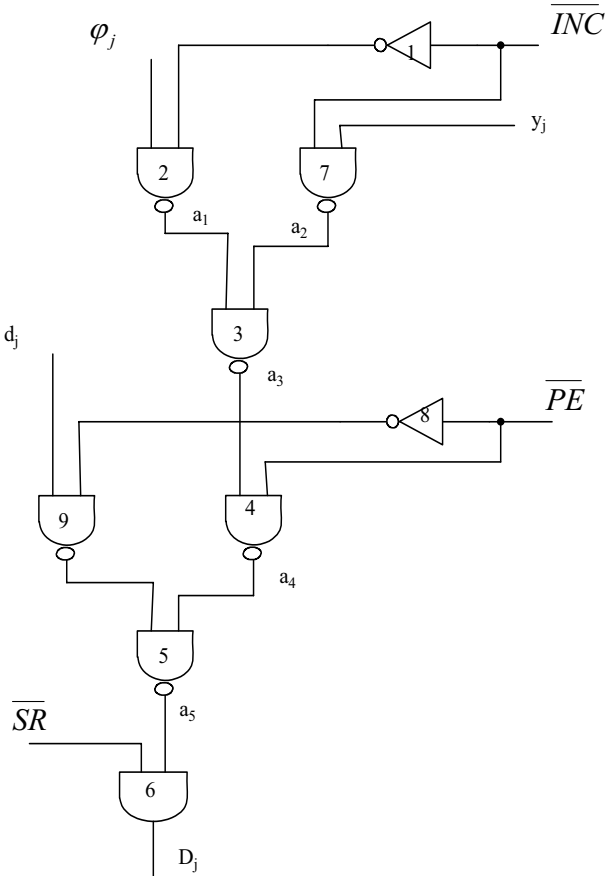


Figure 4. Logic gates implementation.

We will consider the propagation times through logic gates equals ($t_+ = t_{pLH}, t_- = t_{pHL}$), with $t_+ > t_-$. The t_{rec} time parameters will be calculated using the binary values φ_j, y_j . It will be 4 values, notated with $t_{rec}(a)$, where $a = (\varphi_j, y_j)B$.

$$\underline{t_{rec}} = \underline{MAX}[t_{rec}(a)] \quad (7)$$

$$a \in \{0,1,2,3\}$$

If $\varphi_j = y_j = 0$, $\underline{trec}(0) = 0$, hence D_j remains constant on the change of \overline{INC} .

If $\varphi_j = 0, y_j = 1$, the change of $\overline{INC}(H \rightarrow L)$ propagates through the 7,3,4,5,6 circuits, results (8) equation:

$$\underline{t_{rec}(1)} = 2t_+ + 3t_- + \underline{t_{s-u}(D)} \quad (8)$$

If $\varphi_j = 1, y_j = 0$, the change of $\overline{INC}(H \rightarrow L)$ propagates through the 1,2,3,4,5,6 circuits, results (9) equation:

$$\underline{t_{rec}(2)} = 4t_+ + 2t_- + \underline{t_{s-u}(D)} \quad (9)$$

If $\varphi_j = y_j = 1$ the D_j must be constant. Hence $D_{j,n+1} = D_{j,n} = 1$ on \overline{INC} signal change, will result that $\underline{t_{rec}(3)} = 0$.

Really, the situation could be presented in other way, because the (4) structure has static hazard. Indeed, for $\overline{SR} = \overline{PE} = \varphi_j = y_j = 1$, the (1) equation get:

$$D_j = \overline{INC} + \overline{INC} \quad (10)$$

results a hazard generation form. From the $t_+ > t_-$ condition, the signal diagram is showing in figure 5.

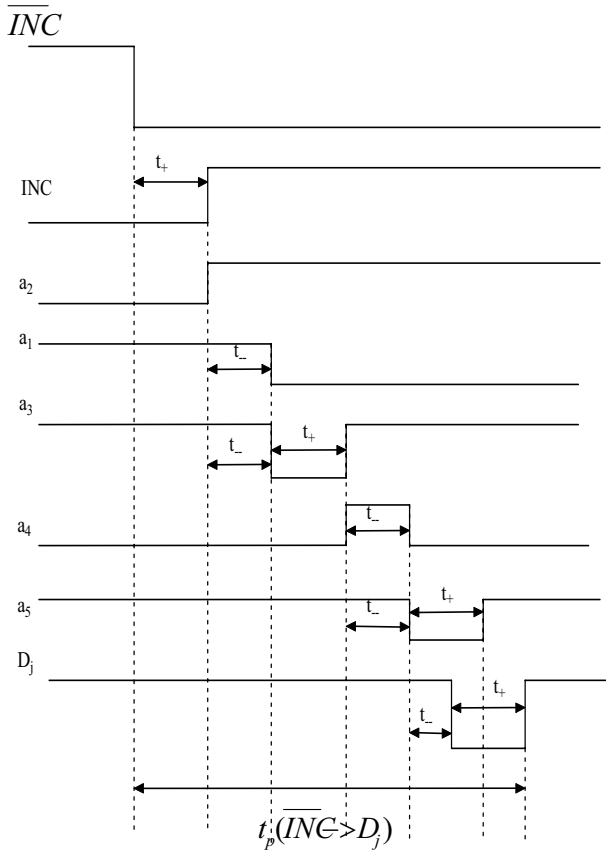


Figure 5. Timing analysis.

Follow the figure 5 result the \overline{INC} timing propagation signal, as (11) equation:

$$t_p(\overline{INC} \rightarrow D_j) = 3(t_+ + t_-) \quad (11)$$

$$t_{rec}(3) = 3(t_+ + t_-) + t_{s-u}(D) \quad (12)$$

From the above analysis, results that t_{rec} , in case of existing the static hazard condition, is different than zero ($\neq 0$). But generally we can't say that is maxim.

In this situation, if we had tried to synthesis the logical structure without static hazard, the costs of the implementation increases.

From the $t_{rec} = \text{MAX}[t_{rec}(0), t_{rec}(1), t_{rec}(2), t_{rec}(3)]$

$$\text{or } t_{rec} = t_{rec}(2) = 4t_+ + 2t_- + t_{s-u}(D)$$

Hence just in static hazard situation, the time set-up for the command remains unfavourable for ($\phi_j = 1, y_j = 0$), in our case.

Examples:

a) TTL circuits implementations:

$$\overline{t_{pLH}} = \overline{t_+} = 22n\text{sec}$$

$$\overline{t_{pHL}} = \overline{t_-} = 17n\text{sec}$$

$$\overline{t_{s-u}(D)} = 20n\text{sec}(CDB - 474)$$

We can say that

$$\overline{t_{sec}} = 4 \times 22 + 2 \times 17 + 20 = 142n\text{sec}.$$

b) CMOS circuits implementations:

$$\overline{t_{pLH}} = \overline{t_+} = 250n\text{sec}$$

for the MMC-4011, $V_{DD} = 5V$

$$\overline{t_{pHL}} = \overline{t_-} = 120n\text{sec}$$

For the MMC-4013 (CBB-D),

$$\overline{t_{s-u}(D)} = 40n\text{sec}$$

$$V_{DD} = 5V$$

$$\overline{t_{rec}} = 4 \times 250 + 2 \times 120 + 40 = 1,28\mu\text{sec}.$$

4. Conclusions

- This paper presents the calculation method for the timing parameters, t_{rec} , t_{rem} for asynchronous control inputs.
- Combinational logical structure of the multifunctional digital circuit may give static hazard, but it's necessary to estimate timing parameters (t_{rec} , t_{rem}).
- Removal time for the control mode, t_{rem} , can be considered null, usually it has negative values.

5. References

- [1] Al.Valachi, R.Silion, M. Timis (2005) *Improvement of FSM Synthesis using MSI and LSI circuits – Advances in Electrical and Computer Engineering – vol 5(12), nr.1(23), ISSN 1582-7445, Suceava.*
- [2] Al. Valachi, Fl. Hoza, V. Onofrei, R.Silion (1993) *Synthesis, Analysis and Testing of Digital Devices - Ed. N.Est.*
- [3] Farzard Nekoogar (1999) *Timing Verification of Application – Specific Integrated Circuits (ASICs) – Pretince Hall PTR*