AC/DC FLY-BACK CONVERTER WITH LOW SWITCHING DELAY

Mihaela MOSCALU, Petre-Daniel IONESCU, Alin MOSCALU
Mihaela Moscalu, "Gr.T.Popa" University of Medicine and Pharmacy, Iasi, str. Universitatii 16, Iasi, mroxyy@yahoo.com
Petre Daniel Ionescu, S.C. FORTUS S.A. Iasi
Alin Moscalu, RAJAC Iasi

Abstract: *This paper refers to a diagram for a simple AC/DC single staged converter, based on fly-back topology. A single switching generates a fast rectified output voltage. Main advantages of this converter are its dimensions and efficiency. Also there is presented a design guide, the line current analysis and analogies with other.*
Keywords: *theoretical wave, fly-back topology, negligible low frequency ripple, fly-back DC/DC converter*

Introduction

Traditional AC/DC diagrams complying to norms referring to the low frequency harmonics' rectifying are comprising two cascaded DC/DC converters connected on the same AC line (Figure 1) [1], [2].
This configuration brings several advantages such as: high power factor, fast rectifying of output voltage, voltage controllable by means of other capacitor's capacity. By the other hand there is the disadvantage of high-costs, large size and efficiency decreased because the voltage's double-processing.
The one-staged systems feed the load with a constant and rectified DC voltage [3], but, in most of cases, the line current is not sinusoidal. In comparison with the two-staged systems there have been developed many strategies focused on the abatement of size and costs, as well as for increasing efficiency, as it follows:

- The enhancing the power's processing - for these systems the main target is efficiency. These systems are based on the splitting of wave shape for the input power, as an attempt to maximize the amount of power processed at one time. Are necessary a number of control loops but the line current is sinusoidal [4];
- The decreasing of switches number – this means the abatement of costs and sizes generated by the switch itself as well as by the control circuit. Because these have a single control loop they are also in charge for keeping a stable rectified output voltage. This technique is applicable to almost all types of cascaded DC/DC converters, with power factor correction. A proper circuit can generate an almost sinusoidal line current;
- Combined topologies – Are converters that perform the power factor correction as well as the output voltage's rectifying and can be obtained by means of combining known topologies and controlling only the output voltage. All these combinations are usually decreasing the number of switches. The key is to obtain simple solutions even if the line current is distorted.

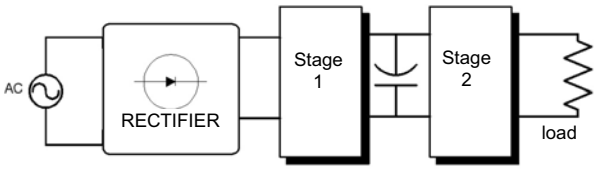

Figure 1. Classic configuration, two stages.

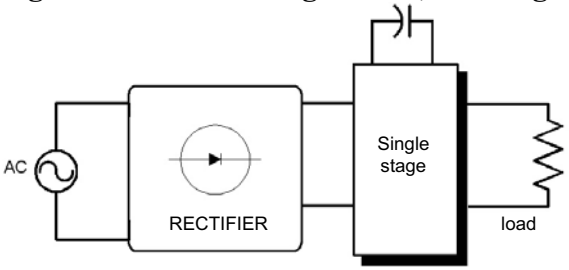

Figure 2. Single-staged configuration.

This paper proposes a single-staged converter able to rectify the output voltage. System's

diagram is given in Figure 3. Converter is derived from a fly-back topology. Because only passive components will be added to it, it will feature only one switch and a single control loop. As Figure 3 shows this converter features two internal inputs, the filtering capacitor being located between them.
The main advantages of this converter are:

- A very simple power stage (low prices and size);
- Power is processed in a single shot (i. e. increased efficiency).

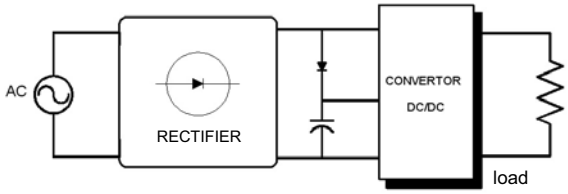

Figure 3. Proposed converter.

A disadvantage is the non-sinusoidal line current. However, the harmonics' content ca be controlled by means of an adequate configuration [2].

Proposed converter

Converter that this paper is proposing is based on a DC/DC converter which is to be added with some additional components, mandatory for AC/DC applications. The control stage is similar to the one featured by a DC/DC converter because the output voltage is the only controlled quantity. Hence, the converter has a very simple configuration. Despite that input current is not controlled, the converter complies to standards regarding the low frequency harmonics.
This converter is derived from known topologies, but descriptions in this paper are the ones corresponding to a fly-back converter. The fly-back DC/DC converter's power stage is given in Figure 4. Converter comprises a transformer T_1, a transistor Q_1, a diode D_1 and the output capacitor C_1.
The performances of the fly-back converter featuring a filtering capacitor C_2: By adding a filter capacitor on the rectifying bridge's output (Figure 4), the converter's input voltage is approximately constant and a well rectified output voltage can be produced. However, it is useful to know, the line current features a high load of harmonics due to its high peak value and its brief switching time.

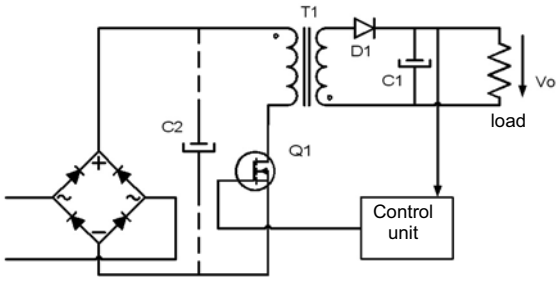

Figure 4. Fly-back converter's power stage.

The fly-back converter's performances without a filtering capacitor: this is a DC/DC converter featuring input voltages on a range between 0 and V_{INmax}, (Figure 4). In an ideal situation it would be proper to use only one such converter in order to supply DC loads from an AC source. Nevertheless, with a single converter of this kind, it is impossible to produce a well rectified voltage on load [3].
Figure 5 shows the theoretical wave shapes for the line current, for a half-cycle, and keeping a constant output power. As it can be seen, because the input voltage is sinusoidal, there would be necessary an almost infinite current at voltage's zero point. Therefore, if a single converter is to be used (without the C_2 capacitor), output voltage drops will occur in passing via zero point [4].

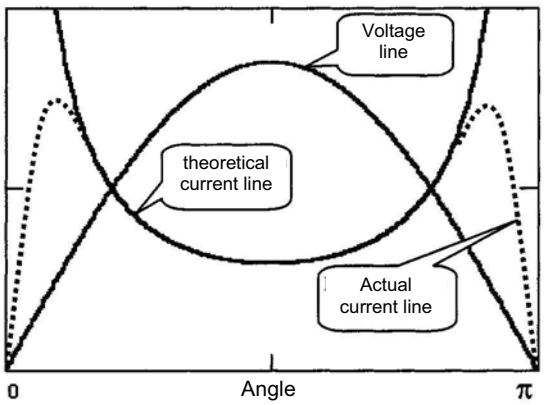

Figure 5. Theoretical and actual line current for a converter without filtering capacitor.

Proposed converter: Combines the two above mentioned converters, making possible the defining of the input current's shape as it is shown in Figure 5. Considering this, the converter has two inputs, one connected to the diode bridge, the other one connected on the filtering capacitor. This capacitor gets loaded up to the peak voltage via a diode.

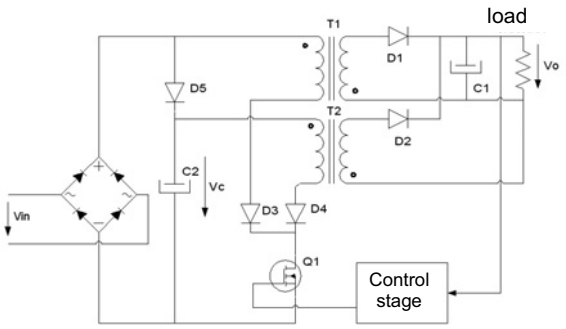

Figure 6. Proposed fly-back double converter: the power stage.

Figure 6 shows the power stage for proposed converter. Basically it is about a fly-back converter (Figure 4) which will be added with some passive components. An auxiliary fly-back branch has also been added, branch comprising transformer T_2 and diode D_2. The input of the auxiliary branch is filtering capacitor C_2 which gets loaded up to the peak input voltage via diode D_5. The amount of power controlled via the auxiliary branch is computed by design. The delivery of 25% of P_o via the auxiliary circuit is an acceptable solution in terms of size and harmonic distortions. Hence, the magnitude of the magnetic component T_2 is low (controls a quarter of P_o) and the magnitude of T_1 is lesser than the one from the original fly-back transformer (controls the remainder of 75% of P_o). Diodes D_3 and D_4 are mandatory in order to avoid to have a current circulating between the two fly-back branches. Both fly-back branches use the same switch Q_1 and the same control loop. Moreover, they also share the output capacitor C_1 (filtering).
The role of this converter is to supply load from both inputs simultaneously, despite that converter is designed to undertake all energy directly from the diode bridge supply. The filtering capacitor C_2 is mainly supplying energy during the line voltage's zero passing.
The filtering capacitor C_2 receives energy from the AC source in the central part of the period. Because the input voltage is high and only a quantum of the power delivered to load is given by energy stored in C_2 (that is 25 % of P_o), the current peaks are also low (1/4 of the current from the converter in Figure 4, with filtering capacitor).
The two converter's transformers can operate in any conduction mode (continuous conduction mode-CCM or discontinuous conduction mode-DCM). The study that follows assumes that both transformers operate in DCM mode.
The main differences of this converter compared to the two-staged systems are:
Advantages:

- low cost and size due to a single switch and a single control loop;
- high efficiency, the output power being processed in a single shot, compared to the two-staged systems, where power is processed twice.

Disadvantages: line current is not sinusoidal.
There is another advantage for this configuration: considering that some loads are needed by standby mode (in computers, VCRs etc.) the transformer T_2 can be used to supply energy in standby mode. Hence, by blocking T_1 (e. g. by means of a relay) in standby mode, the load will be supplied only by T_2, obtaining a huge abatement of losses.
Concluding, it can be said that the fly-back double converter has an acceptable size, and its costs and efficiency are good for low power applications.
The next items will show the converter's performances during switching period, a design guide is given and the line current is analyzed.

The circuit's functioning

The theoretical wave shapes for the converter's main quantities, during a switching period, are given in Figure 7. The converter's operating is explained by assuming that both input branches are in DCM mode.

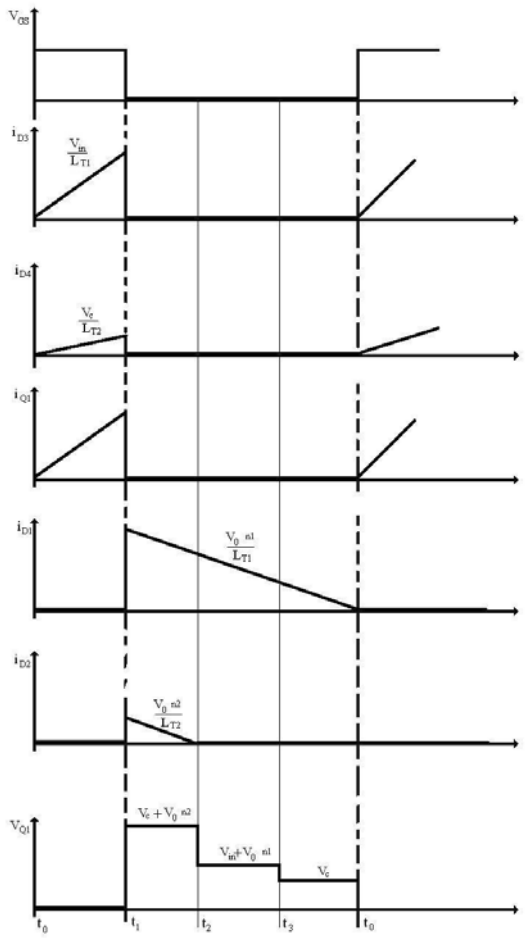

Figure 7. The converter's main wave shapes within a switching cycle.

The t_0-t_1 interval: Switch opens. Both transformers' inductances (T_1 and T_2) are storing energy from rectifying bridge respectively from capacitor C_2. Currents' gradients are varying with the input voltage and with each transformer's inductance. Hence, T_1 with L_{T1} depend on V_{IN} (low frequency rectified sinusoid), whilst T_2 with L_{T2} depend on V_C (voltage almost constant and equal to V_{INmax}). Plus, both currents pass via Q_1. At the end of this period the transformers have already stored the energy that is to be delivered on output.

The t_1-t_2 interval: Switch closes at moment t1. Diodes on converter's secondary side (D_1 and D_2) start to conduct, and transformers are delivering the energy previously stored. Therefore, within this interval, the voltage on transistor Q_1 is the maximum between (V_{IN} + $V_o \cdot n_1$) and (V_C + $V_o \cdot n_2$), where n_1 and n_2 are the transforming coefficients of T_1, respectively T_2. Diodes D_3 and D_4 do not simultaneously conduct, being alternatively blocked. When diode D_3 conducts, D_4 is blocked by voltage from the cathode of D_3, and when D_4 conducts, D_3 is blocked by the voltage in the cathode of D_4.

The t_2-t_3 interval: At moment t_2 the energy within one of the transformers is already released to load (T_2 in our case), this meaning that during this period only one of the transformers is releasing energy towards load (T_1). Voltage on transistor Q_1 in this interval is the maximum between the voltage in transformer T1 (that is V_{IN} + $V_o \cdot n_1$) and the input voltage of the other branch (that is V_C).

The t_3-t_0 interval: At moment t_3 transformer T_1 too releases all its energy towards load. Hence, there will be no more current within circuit. Maximal voltage on transistor Q_1 is the voltage C_2, because it is bigger than the instant voltage from the other input (from the rectifying bridge). At moment t_0 a new operational cycle starts.

Design guide

One of the most crucial issues when designing this converter is to decide the amount of power which is to be delivered to loads on each circuit's branch (P_{MAIN} and P_{AUX}). The power's distribution has a crucial role in terms of line current's harmonics contents and as regards the compliance of this converter to IEC 100-3-2 standard's A or D classes. This can be controlled by means of transformers T_1 and T_2 's inductances (L_{T1} and L_{T2}).

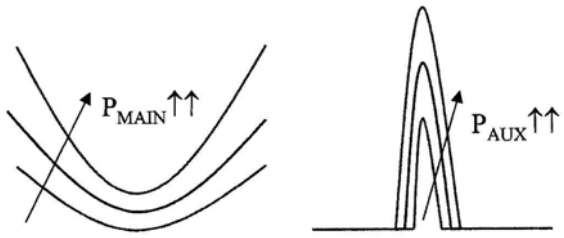

Figure 8. Input currents' wave shapes, on both branches, on a half-period cycle.

Figure 8 shows the input currents' wave shapes, on both branches, on a half-period cycle, function of P_{MAIN} and P_{AUX}. It is to be noticed that the summing of the two currents form the actual line current. Generally speaking, it is a

greater advantage to almost fully deliver power on the main branch, this being a way to abate the peak line currents. If P_{MAIN} is increasing the line current's content of harmonics will increase too, the cause of this being the decreasing of input current on the auxiliary branch. Thus it is easier to avoid the standard D class, which is much more restrictive. Class A imposes only the absolute limits for some power levels. By assuming that voltage on storage capacitor (Vc) is constant, with a negligible ripple, the equations for the main converter's quantities can be obtained.

Because both converter's transformers work in DCM mode, the input current's peaks within each transformer (i_{D3} and i_{D4} – Figure 7) can be easily computed for one switching cycle:

$$I_{LT1,max}(\omega t)=\frac{V_{in}(\omega t)}{L_{T1}\cdot f}\cdot d(\omega t) \quad (1)$$

$$I_{LT1,max}(\omega t)=\frac{V_C}{L_{T2}\cdot f}\cdot d(\omega t) \quad (2)$$

where $V_{IN}(\omega t)$ is the instant line current, $d(\omega t)$ is the filling factor, L_{T1} and L_{T2} are transformers' magnetic inductances and f is the converter's switching frequency.

With average values, within one switching cycle it is possible to obtain the evolution of input current at low frequencies, as it can be seen from the equations below:

$$I_{LT1,AVG}(\omega t)=\frac{V_{in}(\omega t)}{2\cdot L_{T1}\cdot f}\cdot d^2(\omega t) \quad (3)$$

$$I_{LT2,AVG}(\omega t)=\frac{V_C}{2\cdot L_{T2}\cdot f}\cdot d^2(\omega t) \quad (4)$$

Multiplying current with voltage, we can compute the input powers on each branch:

$$P_{LT1,AVG}(\omega t)=\frac{V_{in}^2(\omega t)}{2\cdot L_{T1}\cdot f}\cdot d^2(\omega t) \quad (5)$$

$$P_{LT2,AVG}(\omega t)=\frac{V_C^2}{2\cdot L_{T2}\cdot f}\cdot d^2(\omega t) \quad (6)$$

The sum of these powers should equal the output power on each switching cycle, for a proper supply of load:

$$P_{LT1,AVG}(\omega t)+P_{LT2,AVG}(\omega t)=P_0=\frac{V_0}{R} \quad (7)$$

By replacing $V_{IN}(\omega t)$ with $V_{IN,max}\cdot\sin(\omega t)$ and V_C cu $V_{IN,max}$ in equation (7), it is possible to obtain an equation for the filling factor, as it can be seen below:

$$d(\omega t)=\frac{V_0}{V_{IN,max}}\cdot\sqrt{\frac{2\cdot L_{T2}}{RT\cdot\left(1+\frac{L_{T1}}{L_{T2}}+\sin^2(\omega t)\right)}} \quad (8)$$

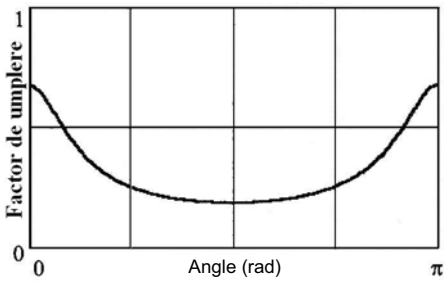

Figure 9. An example for the filling factor's evolution on a half-cycle.

The filling factor's theoretical evolution, according to equation (8), is given in Figure 9, for L_{T1}/L_{T2} = 0,1. Is maximal when input voltage is almost zero, when only the auxiliary branch will deliver energy towards load. Once the filling factor is computed the input power's wave shapes (P_{MAIN} and P_{AUX}) are easily to be deduced from equations (5), (6) and (8). Equations (9) and (10) are giving the power on each branch:

$$P_{MAIN}(\omega t)=\frac{V_o^2}{R}\cdot\frac{\sin^2(\omega t)}{\frac{L_{T1}}{L_{T2}}+\sin^2(\omega t)} \quad (9)$$

$$P_{AUX}(\omega t)=\frac{V_o^2}{R}\cdot\frac{L_{T1}}{L_{T2}}\cdot\frac{1}{\frac{L_{T1}}{L_{T2}}+\sin^2(\omega t)} \quad (10)$$

Figure 10 shows the power's wave shapes, according to equations (9) and (10), for the specific case of a 100W converter with L_{T1}/L_{T2}=0,1. It can be noticed that the auxiliary branch has the role to supply the load when voltage goes through zero.

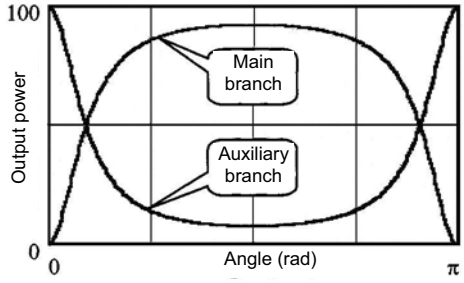

Figure 10. Power distribution between branches in a half-period.

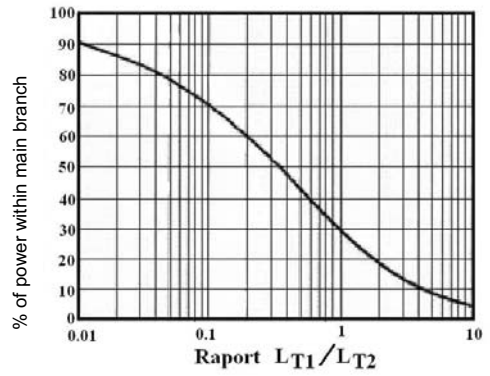

Figure 11. Power controlled by main branch function of L_{T1}/L_{T2} ratio.

As it can be seen from previous equations, the L_{T1}/L_{T2} ratio is the converter's most important parameter (when working in DCM mode). Making average for equations (9) and (10) on a period we can compute the amount of power delivered via each branch, as it can be seen in Figure 11. A low L_{T1}/L_{T2} ratio means more power on main branch.

Within our converter the filling factor is varying with the double of line frequency, as it can be seen in equation (8); the filling factor gets maximal for $\omega t = \frac{\pi}{2}$. The filling factor's variation is a crucial design parameter. Making equation (8) specific for extreme values, can be obtained the ratio between the maximal and minimal filling factor this way:

$$\frac{d_{MAX}}{d_{MIN}} = \sqrt{1+\frac{L_{T1}}{L_{T2}}} \qquad (11)$$

It can be noticed that this ratio depends only of the L_{T1}/L_{T2} ratio for converters operating in DCM. Because it is not recommended to have a big variation of the filling factor, more power would be needed on the main branch.

Analysis of line current

The L_{T1}/L_{T2} ratio plays a very important role in terms of harmonics content within line current. A high L_{T1}/L_{T2} ratio means a bigger peak current required by the storage capacitor C2 in the middle of a half-cycle, what leads to an increase of the harmonics content. By the other hand a very low L_{T1}/L_{T2} ratio gives a bigger current on the main branch when the line voltage goes through zero. In this case too the harmonics content is high.

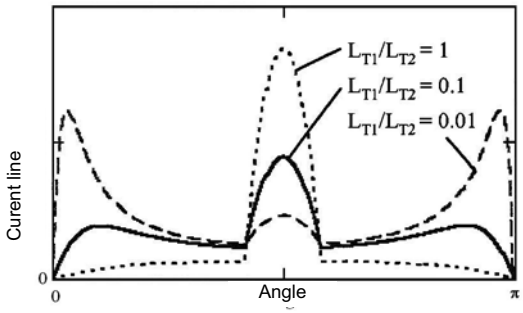

Figure 12. Line current for various L_{T1}/L_{T2} ratios in a half-period.

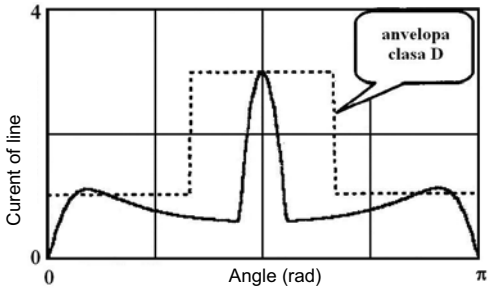

Figure 13. Line current and D class envelope in a half period.

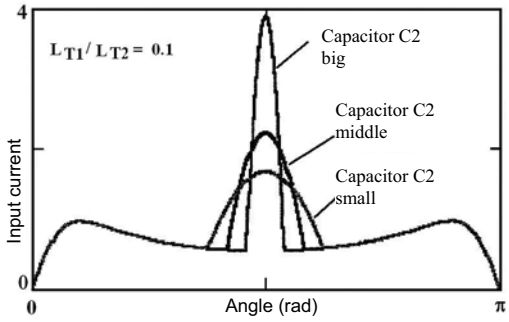

Figure 14. Line current for a half-period for various values of capacitor C2.

It has been checked that the best solution, in terms of harmonics content, is to have a L_{T1}/L_{T2} ratio of approximately 0,1 (assuming that conduction angle of diode D5 is of 30º). For this ratio the amount of power distributed by main branch is approximately 70%. Figure 12 shows the theoretical line currents for different values of L_{T1}/L_{T2} ratio

Moreover, due to the line current's specific shape, with a proper configuration, it is easy to

avoid the IEC standards D class, being possible to make the device compliant to norms for medium powers. By example, with a conduction angle of 30º for D5 and a ratio $L_{T1}/L_{T2}<0,2$, the current wave shape complies to A class. The theoretical wave shape is shown in Figure 13. It complies to D class even if filtering capacitor gets loaded with relatively big peak currents.
Next to theoretical calculations for harmonics contents for line current, it can be seen that the lowest harmonics content is obtained for a ratio $L_{T1}/L_{T2} \approx 0,1$. The amplitude of the third harmonic is low, and, typically, there is to be computed a fifth harmonic, the most restrictive one. For a 100W output power, the harmonics content is far away from the limits foreseen by IEC 100-3-2, therefore the line current is complying to the limits for big powers. For efficiency reasons, the power specifications for this converter must be of 100-200W.

The current peak wave shape is intensely influenced by capacitor C2. Figure 14 shows the effect of changing of this capacitor. A high capacity for C2 leads to a lesser conduction angle, that is a higher harmonics content, but do not affect the powers distribution between branches, parameter which depends only on L_{T1}/L_{T2} ratio. The explanation is that on has been assumed that voltage on storing capacitor is constant, with a negligible low frequency ripple.

Plus, the magnitude of the capacitor within this diagram (capacitor C2 in Figure 6) is lower compared to a capacitor from a regular fly-back converter (the capacitor C2 in Figure 4), because via these capacitors is filtered a lower current ripple (approximately ¼). This is in fact an advantage because converter's size and costs get decreased. In order to test these theoretical results and performances of this system with PSpice soft the main converter's wave shapes have been simulated: the filling factor, the input current on each branch and the power.
It can be noticed the similitude between the theoretical waves shapes (Figures 9, 10, 12) and the simulated wave shapes (Figure 15).

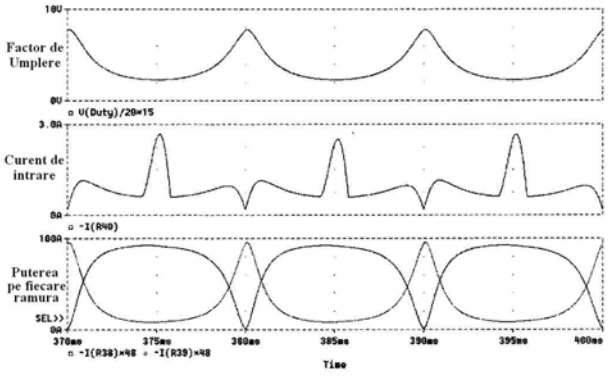

Figure 15. Evolution of filling factor, line current and power.

Conclusions

This paper adopts a new diagram for a simple, single-staged and single-switch AC/DC converter. This converter generates a fast rectified voltage, using a single switch and a single control loop.
Converter is based on classic fly-back topology, being fitted with an additional branch. This branch features a storage capacitor which receives energy directly from the AC supply. This energy is released towards output only when input voltage passes through zero, using the same fly-back converter's switch.
The main advantages of this converter, compared to the two-staged version, are the simple configuration, the small size and its efficiency. Moreover, it is one of the simplest solutions among the single-staged devices. The line current is not sinusoidal, but complies to limits imposed by IEC 100-3-2 norms, due to its special wave shape. With a proper circuit, this converter complies to A class within these norms, for medium powers (cca. 500W).
Proposed concept can be extended to other known topologies such as Boost, SEPIC, Forward etc. Benefits brought by this converter have been certified also by means of presented simulations.

References

[1] Diaconescu, M.P. and I. Graur (1996). *Convertoare statice*, Editura „Gh. Asachi”, Iaşi.

[2] Lucanu, M. (1997) *Convertoare performante de curent continuu*, cap. 4.4, pp. 179-186, pp. 207-216, Editura Printech, Bucureşti.
[3] R. Redl (1998) *An economical single-phase passive power-factor corrected rectifier*, pp. 454-460, IEEE Appl. Power Electron. Conf. (APEC).
[4] R. Redl, L. Baslogh, N. O. Sokal (1994) *A new family of single-stage isolated power factor corrector with fast regulation of the output voltage*, pp. 1137-1144, IEEE Power Electron. Spec. Conf.(PESC)
[5]* * * http://www.etc.utt.ro/ea/courses/docs

Appendix

Starting with 01.01.2001, in EU countries, new standards enter in force, standards that will define the conditions that must be fulfilled by currents absorbed from supply sources. Considering this, the input filters comprised within feeding sources must be designed in order for input current to be compliant to standards IEC 1000-3-2 or IEC 1000-3-4 and CISPR 11 [5]. Standards IEC 1000-3-2 and IEC 1000-3-4 are defining the maximal admissible level for low frequency harmonics, precise limits being settled for each input current's harmonic, from the 2nd order harmonic up to 40th order harmonic.
The IEC 1000-3-2 standard defines these limits for equipments with nominal input current lesser than 16A. The standard IEC 1000-3-4 defines these limits for equipments with nominal input current greater than 16A.
Equipments classification for standard IEC 1000-3-2 is done in four classes as it follows:
Class A: Balanced 3-phase equipment and all other equipment except those in one of the following classes.
Class B: Portable tools
Class C: Lighting equipment including dimming devices with input active power above 25W.
Class D: Equipment having an input current with "special wave shape" and a fundamental input active power between 75 and 600W. This is the "high crest factor" waveform; e.g. single-phase rectifier input current waveform.
The limits of harmonics for each phase of the line current are shown in Table 1. Note that the limits are absolute, i.e. not related to power ratings of equipment. The limits are applicable to steady state harmonic currents.

Table 1. The limits of harmonics for each phase of the line current

Harmonic order (n)	**Class A max permissible harmonic current (A)**	**Class B max permissible harmonic current (A)**
Odd harmonics		
3	2.30	3.45
5	1.14	1.71
7	0.77	1.155
9	0.40	0.60
11	0.33	0.495
13	0.21	0.315
15<=n<=39	2.25/n	3.375/n
Even harmonics		
2	1.08	1.62
4	0.43	0.645
6	0.30	0.45
8<=n<=40	1.84/n	2.76/n