LOW OUTPUT OFFSET CURRENT-MODE FREQUENCY TRIPLER

Doru E. TILIUTE
"Stefan cel Mare" University of Suceava
str. Universitatii nr.13, RO-720229 Suceava
dtiliute@eed.usv.ro

Abstract. *In this paper we present an improved current-mode sinusoidal frequency tripler characterized by a very low output offset. The previous reported circuit leaks by the presence of a substantial output DC component which has to be canceled by means of additional circuits. These errors arise as a result of the circuit's topology or/and of the non-ideal devices behavior. The proposed solution reduces dramatically the output-offset current of a frequency tripler to values very close to zero.*
Keywords: *translinear circuits, current-mode, frequency multiplier, DC errors.*

Introduction

Nowadays translinear circuits have a wide deployment in various integrated circuits like transconductance operational amplifiers [1,2], logarithmic amplifiers [3], current-mode feedback amplifiers, [4]. In the past few years a new class of applications were found for these circuits, namely the frequency multiplication. Frequency multiplication is an important function, mainly used in telecommunication and instrumentation systems. It is found in frequency synthesis, oscillators and modulation circuits. The conventional methods to achieve sinusoidal signals, whose frequency equals a multiple of a fundamental one, use the harmonic frequency filtering, the piecewise-linear voltage sawtooth operator or the fundamental-rejecting feedback. Despite this, the frequency multiplication has rarely been approached in literature as compared to other useful applications and only a few achievements have been reported [5,6]. In a previous paper [7] two new circuits topology, which perform frequency doubling and frequency tripling respectively, have been introduced. Both of them require a slight adjustment of the output current by means of additional current sources in order to reach high spectra purity and a low DC component. We will further discuss the frequency tripler circuit and the solution proposed to eliminate the DC component of the output current.

The basic circuit

The basic circuit is reproduced in figure 1.

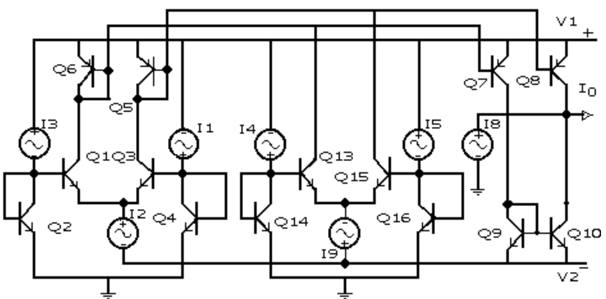

Figure1. Translinear frequency tripler.

We will not further discuss the circuit functioning that has already been done in [7], we will only present the principle and the results. The principle consist in the implementation of the trigonometric identity:

$$\sin 3\alpha = \sin\alpha + 2\sin\alpha\cos 2\alpha \tag{1}$$

using translinear circuits. This is possible by means of a beta-insensitive Gilbert cell with two current sources, one of them having the fundamental frequency ω (I1 / I3) and the second with double frequency, 2ω, (I2 / I9) and an algebraic circuit to perform elementary operations as addition and subtraction. In figure 1 the source of fundamental frequency is represented by two independent current sources with the same amplitude but in phase opposition.

Because each of the Gilbert cell outputs includes a component of double frequency, we choose to eliminate it by employing two identical Gilbert cells connected as shown in figure 2.

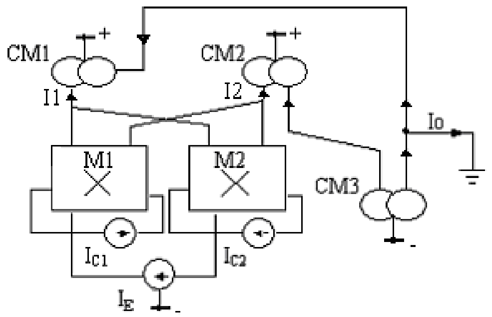

Figure 2. Block scheme of circuit from fig.1.

It was shown [7] that currents i_1 and i_2 from figure 2 could be expressed as follows:

$$i_1 = I_{EB} - \frac{I_a^2}{I_B}\sin\omega t\cos 2\omega t \quad (2)$$

$$i_2 = I_{EB} + \frac{I_a^2}{I_B}\sin\omega t\cos 2\omega t \quad (3)$$

where Ia is the magnitude of variable components and I_{EB} and I_B are two bias currents. Assuming that all current mirrors have unity gain, the output current is:

$$i_o = i_2 - i_1 = \frac{2I_a^2}{I_B}\sin\omega t\cos 2\omega t \quad (4)$$

Comparing with equation (1) we notice that by simply adding the component with the fundamental frequency

$$\frac{I_a^2}{I_B}\sin\omega t \quad , \quad (5)$$

we obtain frequency triplication:

$$i_o^{'} = \frac{I_a^2}{I_B}\sin\omega t + \frac{2I_a^2}{I_B}\sin\omega t\cos 2\omega t = \frac{I_a^2}{I_B}\sin 3\omega t \quad (6)$$

Sources of errors

The two Gilbert multipliers M1 and M2 have identical structures and deploy bipolar transistors of the same type, so we are right in supposing that they will not produce any asymmetry in the output current.

Unlike this, it is easy to notice that the addition/subtraction circuits, built with current mirrors CM1 to CM3, are asymmetric and susceptible to produce unwanted components in the output current. Moreover, as it can be seen in figure 1, the current mirrors use transistors of different type, namely CM1 and CM2 use PNP transistors since CM3 uses NPN transistors. This is a new source for additional asymmetry.

In the basic circuit the current mirrors are regular ones, characterized by the gain k,

$$k = \frac{\beta}{\beta + 2} < 1 \quad (7)$$

where β is the current gain of the bipolar transistors (all transistors are supposed to be identical, with the same β) . This is an important factor which alters the circuit overall gain and the output current components.

For the circuit reproduced in figure 1 and the references of currents in figure 2, a new DC component occurs, the offset component, whose value is given by equation (8):

$$I_{OFF} = \frac{-\beta}{(\beta+2)^2} I_{EB} \quad . \quad (8)$$

At the same time the magnitude of variable component becomes smaller, with the exact value:

$$\frac{\beta(2\beta+3)}{(\beta+2)^2}\frac{I_a^2}{I_B} \quad . \quad (9)$$

The role of the current source i_8 source is to nullify the DC component and to supply the suitable variable component for the frequency tripling.

SPICE simulations of the basic circuit yield the following values for the output components: I_{OFF} = -24 uA, i_O= 93 uA; the DC component is far different by the theoretical one which is -2.11uA, since the variable component with triple frequency is quite close to I_V=81.2 uA, which was also theoretically determined. The cancellation of the DC component requires a DC current source connected to the output node of the circuit (included in I8 source in figure 1), with identical magnitude and opposite sign, which may be an extra complication of the circuit. All simulations and computations were made with following values of source currents: I_{EB}=0.22 mA, Ia=0.1 mA, I_B=0.12 mA

Possible improvements

As we already shown above, one of errors source is the circuit asymmetry. This could be avoided by using a fully symmetric circuit having the block diagram reproduced in figure 3.

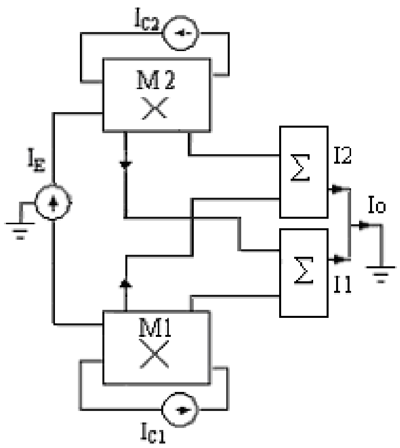

Figure 3. Block scheme of fully symmetric circuit.

The circuit consists in two complementary current multipliers and in a symmetric algebraic circuit. However, the integrated PNP and NPN transistors have very different values of parameters that can lead to a non-zero output offset. Another solution, described bellow, is the deployment of better performance current mirrors instead of regular ones. We must mention that this solution changes the translinear nature of the circuit converting it into a current-mode circuit. There is no problem with that as long as the translinear circuits represent a particular class of current-mode circuits, while the current-mode operation is the one that dictates the circuit special behavior. In bipolar technology there are such current mirrors, namely Wilson mirror, EF-augmented (EFA), cascode and Wildar (Widlar). In MOS technology there are also some topologies of MOS current-mirrors: simple, cascode and Wilson. The diagram of bipolar Wilson mirror EFA mirror and cascode mirror are shown in figure 4.

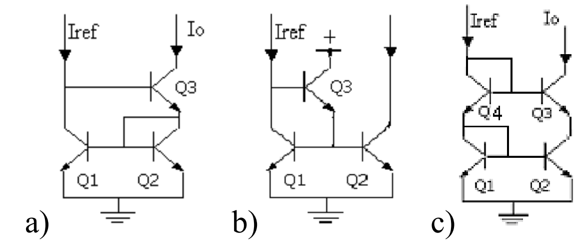

Figure 4. a) The Wilson mirror b) EF-augmented mirror and c) cascode mirror.

Only first two current mirror types provide a good mirroring ratio, close to unity in a wide range of beta values according to equation (10); the cascode mirror is less suitable for our purpose because it has a low current gain and reduces the voltage swing of output stage.

$$k = 1 - \frac{2}{\beta^2} \cong 1 \qquad (10)$$

However, because the Wilson mirror exhibits larger output impedance due to the weak positive feedback effects, and thus being much closer to the ideal current source, we will further discuss this case only. Therefore, with the value given in equation (10) we can expect a better response from the circuit. Indeed, renewing the errors computation with the new gain expression, the following values are found for the offset current and the variable component magnitude:

$$I_{OFF} = \frac{-2(\beta^2 - 2)}{\beta^4} I_{EB} \qquad (11)$$

$$\frac{2(\beta^2 - 1)(\beta^2 - 2)}{\beta^4} \frac{I_a^2}{I_B} \cong 1 \qquad (12)$$

With eqn. 11 and 12 we can estimate the numeric values of the offset current and the variable component magnitude for the same currents of the sources as in the basic circuit example: I_{OFF}=0.043 uA, I_V=83.3 uA.

The modified version of the tripler circuit is depicted in figure 5. Up to the basic circuit only three additional transistors have been included in order to achieve the Wilson mirrors.

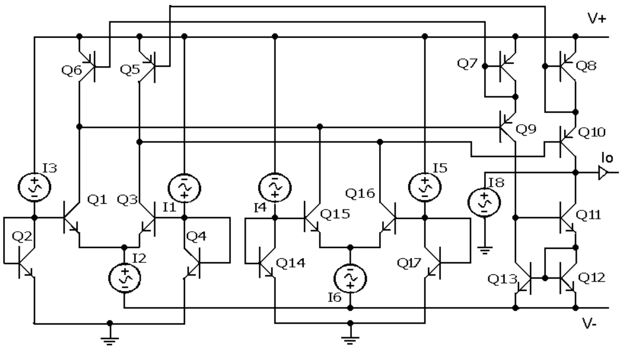

Figure 5. Improved current-mode frequency tripler.

MOSFET current mirror solution

MOSFET transistors have no power consumption on the gate input and this is a reason why we should take them into account, despite the worse frequency response comparing to the bipolar transistor. The scheme of simple CMOS mirror is given in figure 6. For identical transistors the output current Io equals the reference current Iref.

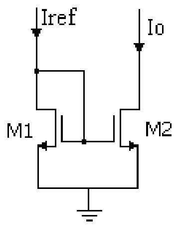

Figure 6. Simple NMOS current mirror.

The circuit topology remains the one depicted in Figure 1, the only difference consisting in the replacement of bipolar current mirrors with simple MOS ones. Renewing the computation of the DC component in this case, we find that it should be zero.

Simulated results

The simulations were made for both circuits, with bipolar Wilson mirrors and MOS simple mirrors, in the same conditions as the basic circuit. Figure 7 displays the transient response of the circuit. The measured amplitude of the output signal is 82.2 mA, result that matches well the theoretically estimated value 83.3 mA. Furthermore, the measured offset component is –0.58 uA, which is over 10 times greater than the one estimated in ideal conditions, but over 40 times smaller than the offset of the basic circuit.

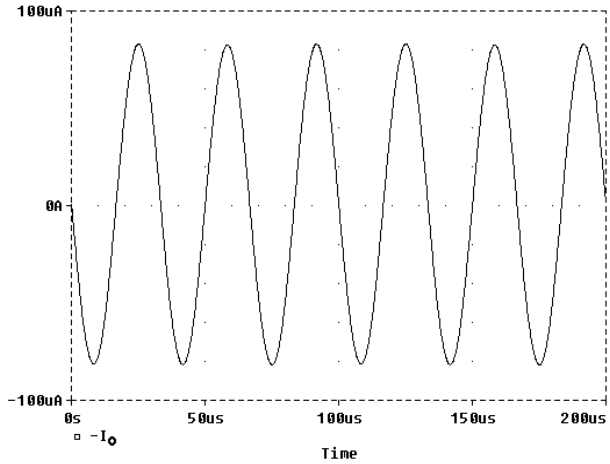

Figure 7. Transient response of the tripler from Fig.5.

The ratio between the amplitude of the output current and the offset current is by far favorable to the last circuit: 152.2 vs. 3.83. Slight changes can be differentiated in the output current spectra, concerning the purity.

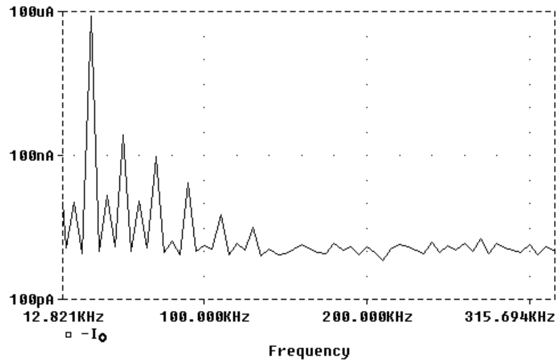

Figure 8. Frequency spectra of output current (Wilson mirrors).

Figure 8 displays the magnitude of the main harmonic components; a ratio of 49.8dB has been measured between the third harmonic - the useful one - and the fifth harmonic that has the highest value among all unwanted components. The rejection of the fundamental is a bit smaller as compared to the basic circuit, (52.6 dB vs. 59.8 dB). As for the circuit bandwidth, it remains unchanged, as it can be seen in figure 9. The employment of EFA current mirrors led to worse results regarding the offset current, since the spectra and the frequency response remained practically unchanged.

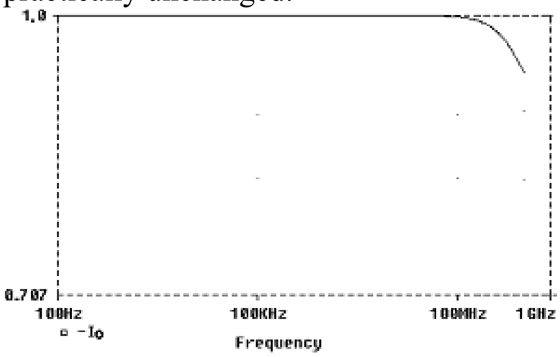

Figure 9. Frequency response of the tripler circuit from Fig.5.

During simulations, each EFA mirror had a resistor of 300 ohms in the emitters of Q1-Q2 transistors.

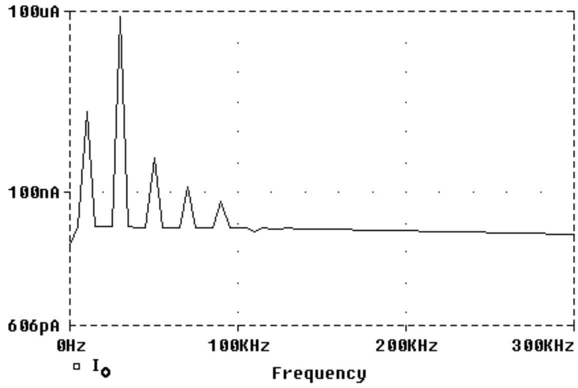

Figure 10. Frequency spectra of the output current (MOS mirrors).

As for the MOS current mirrors the simulations confirmed the better behavior of the circuit regarding the DC component. Unfortunately, in this case, the rejection of the fundamental and the fifth harmonic is lower compared with all the bipolar implementations. On the other hand, the highest harmonics are practically eliminated, as can be seen in figure 10.

Table 1. Comparative results

	Regular	EFA	Wilson	MOS
Offset	24 uA	11 uA	0.043 uA	18 pA
Iv	93 uA	83.4 uA	82.2 uA	82.4 uA

All these results are presented in table 1, alongside the basic circuit ones, in order to facilitate the comparison**.**

Conclusions

We tried to show that a basic translinear circuit that has the property to achieve frequency triplication without the need of resonant circuits could be optimized from the viewpoint of the DC component magnitude of its response. The analysis of the circuit topology evidenced the possible source of errors. The adoption of an improved solution for the arithmetic circuit, by replacing regular current mirrors with Wilson current-mirrors or MOS current mirrors, led practically to the cancellation of the offset current. Depending on application, pondering the advantages and the drawbacks of each solution, we can adopt the better one. Both in Wilson and MOS current mirror solutions, due to the very low level of the offset current, no external trimming circuits are required.

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