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A NEW LOW VOLTAGE FULLY DIFFERENTIAL LINE DRIVER FOR HIGH-SPEED DATA TRANSMISSIONS

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Abstract. *In this paper, a new low voltage, fully differential line driver for high-speed data transmissions, in a 0.13 μm CMOS process, is presented. The line driver power consumption is 46mW from a 1.5V supply and drives a 75Ω resistive load. It has a good linearity and a 345MHz bandwidth at -3dB with phase margin of 60°. The structure used for the line driver is based of two stages, an input folded cascode preamplifier built by an input differential pair with NMOS transistors, and also a class AB output stage. Both stages have independent common-mode feedback loops. The line driver presented in this paper has also a resistive feedback from output to input, which leads to a significant decrease of input voltage swing and distortions. The simulations made in 0.13 μm CMOS process confirm the theoretically obtained results.*
Keywords: *line driver, folded cascode, data transmission, CMOS, linearity, THD, common-mode feedback*

1. Introduction

There is great interest in transmitting high-speed data over coaxial and unshielded twisted pair (UTP) cables due to their availability and low-cost. However, there are few problems, such as linearity, for circuits and systems designers. An important challenge is to design a linear line driver, which represent the last stage of a data transceiver.
In the previous designs, such as ISDN [1] – [3], due of low-speed data transmission, extra feedback loop was applied to a class AB stage in addition to the feedback loop of the architecture. This supplementary feedback loop has the role to decrease distortions of the class AB stage, which must deliver high current to a low resistance load. However, in high-speed data transmission, two feedback loops cause instability due to the large phase shift. For modern line drivers [5] – [7] this local feedback loop is omitted. It is very important to maintain open-loop gain up to high frequencies, in order to attenuate the distortion by feedback. All of the above architectures use folded cascode amplifier and class AB output stages, and feedback is obtained by a differential stage. The standard block schematic of the above line drivers is presented in Fig. 1 [1].

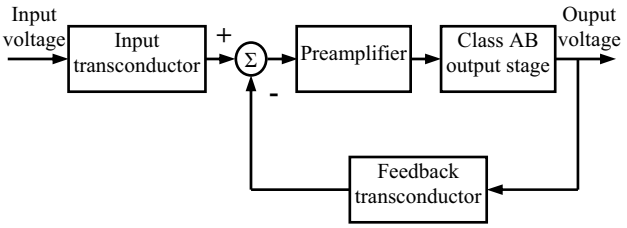

Figure 1. Bloc schematic of the conventional line driver.

It is noticed the fact that the input differential stage is outside of the feedback loop, which allows to apply a large input voltage at their gates. This causes great distortions which are introduced into the circuit and are not attenuated by feedback. In addition, the feedback transistors operate with considerable voltage swing at their inputs which causes further distortions. In order to reduce these architectures' distortions, a fraction of the output voltage is applied to the feedback loop transistors. For low frequencies, these distortions can be reduced by feedback, but at high frequencies, where the open-loop gain is reduced, the distortions become more significant [1].
In the architecture used in this paper, proposed in [1], the feedback differential pair is excluded, employing resistive feedback to reduce distortions. In this paper, the input differential pair of the folded cascode preamplifier is built

by NMOS transistors, which perform better in frequency than PMOS transistors used in previous designs from literature [1]. In addition the line driver proposed in this paper has a lower power consumption from a 1.5 V supply, small distortions and a performing frequency response.

2. Principle block schematic of the line driver

The principle block schematic of the line driver proposed in this paper is presented in Fig. 1 [1].

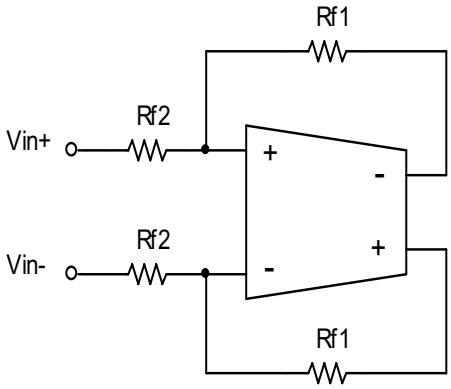

Figure 2. Simplified schematic of the line driver.

In this architecture, the input transistors are included in the feedback loop. This causes reduced input voltage swing and distortions. The differential feedback is realized by R_{f1} and R_{f2} resistors. Therefore, feedback transistors and their corresponding distortions are eliminated. Moreover, because of using a fully differential architecture, common-mode perturbations – such as substrate or power supply noise are rejected. In addition even order harmonics are also eliminated [1]. As consequence, by using a resistive differential feedback in the line driver, the main part of the conventional designs problems reported in literature are solved.
Considering that the amplifier has a high gain, the over-all gain of the line driver is given by the following equation [1]:

$$\frac{V_{out\,diff}}{V_{in\,diff}} \approx -\frac{R_{f1}}{R_{f2}} \qquad (1)$$

The ratio of the two resistors and the closed-loop gain is independent of temperature and process variations. For the line driver proposed in this paper, the closed-loop gain is chosen as equal to 2.

3. Electrical schematic of the proposed line driver

The complete electrical schematic of the proposed line driver is shown in Fig. 3. In order to simplify the representation, the biasing circuits are not presented. The proposed line driver is formed by two main stages and their corresponding common-mode feedback loops:

1) *Folded cascode input preamplifier* (Fig. 3.a)) built by M_1–M_{14} transistors; common-mode feedback loop of preamplifier (Fig. 3.b)) built by M_{15} – M_{25} transistors;

2) *Class AB output stage* (Fig. 3.c)) built by M_{101}, M_{102}, M_{201}, M_{202} transistors and R_{S1}, R_{S2} resistors; common-mode feedback loop of the output stage (Fig. 3.c)) built by M_{301}-M_{304} transistors and R_{C1}, R_{C2} resistors.

Both stages are fully differential, so their output common-mode level must be well controlled. In this work instead of applying an overall common-mode feedback, we used two separate feedback circuits in the two stages [1].
R_{f1} and R_{f2} resistors form the differential feedback network of the line driver and are chosen **300Ω** and **150Ω**, respectively. R_{S1} and R_{S2} resistors are used to provide a dc shift between the gate voltages of NMOS and PMOS transistors. These were chosen as **100Ω** and **600Ω**, respectively.

3.1. Folded cascode input preamplifier

Folded cascode input preamplifier has an input differential pair built by NMOS transistors (M_1 and M_2). By using NMOS transistors for this input differential pair allows selecting a 700mV common-mode voltage for the proposed circuit. In addition, the NMOS transistors have a better frequency response than PMOS transistors. This aspect improves the frequency performances of the proposed line driver.

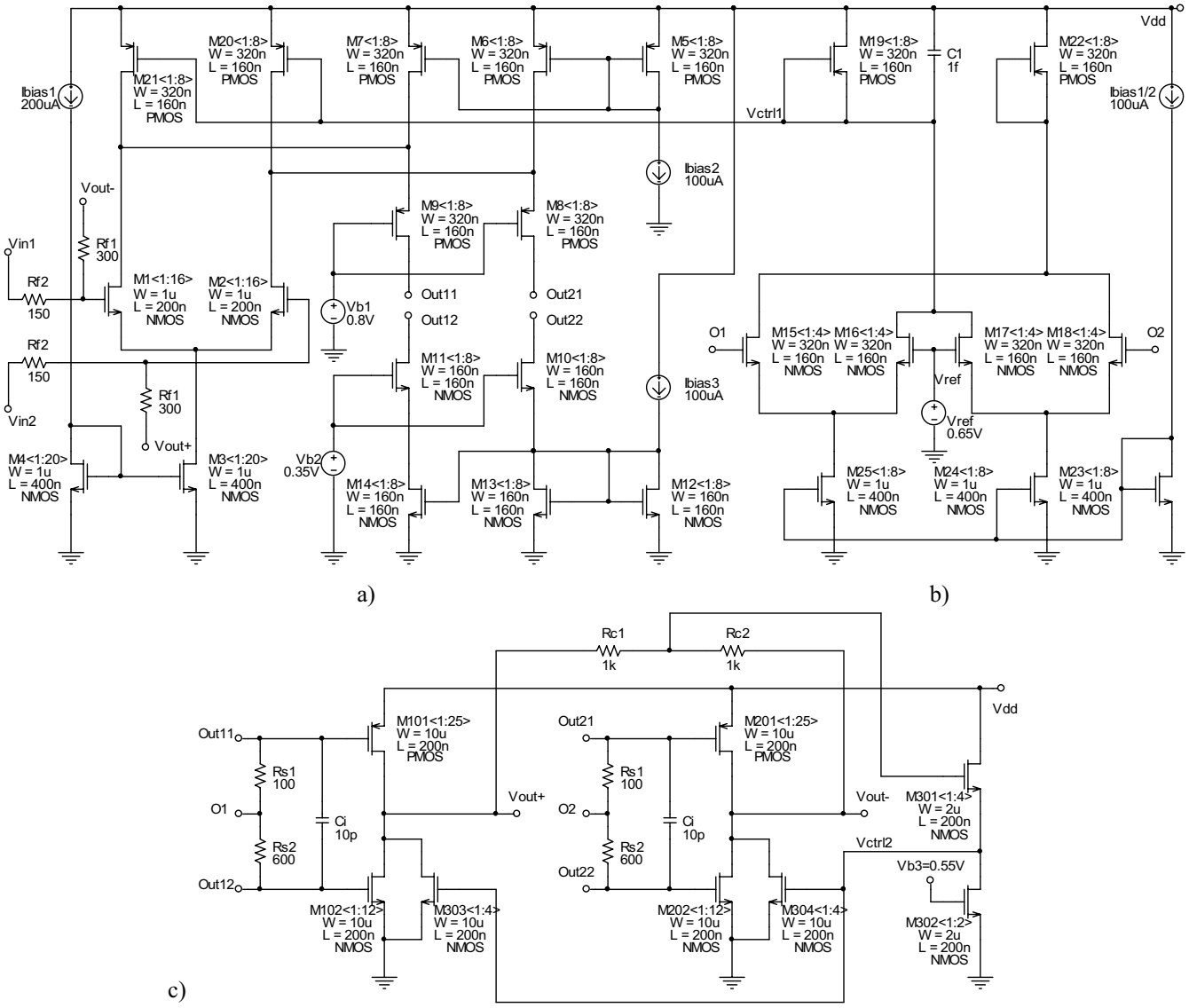

Figure 3. Electrical schematic of the proposed line driver: a) Input folded cascode preamplifier; b) Common-mode feedback circuit of the preamplifier; c) Class AB output stage and its common-mode feedback circuit.

For the proposed circuit, two separate feedback circuits are used in the two stages, instead of using an overall common-mode feedback which is usually slow. This gives an important distortion lowering [1], [7].

The common-mode feedback of the preamplifier is shown in Fig. 3.b). If the output common-mode voltage differs from V_{ref}, the current of M_{15} and M_{18} transistors change, and this leads to increase or decrease of V_{ctr1} voltage. Then this voltage is applied to M_{20} and M_{21} transistors, whose currents can control output common voltage [11].

The second common-mode feedback (of the class AB output stage) is very simple and fast because of the small loop [7].

Resistors R_{C1}=R_{C2}=**1kΩ** detect output common-mode voltage and then this voltage is fed to M_{303}-M_{304} after a dc-shift. Without a dc-shift, devices M_{303}-M_{304} enter the linear region when the output voltage swing is large [7]. So, the common-mode feedback gain decrease and it

doesn't work. This causes large distortions in the output voltage.

3.2. Class AB output stage

The second stage of the line driver is class AB power amplifier shown in Fig. 4.
To analyze this stage, one should consider the schematic shown in Fig. 4.a), which can be modeled as Fig. 4.b) shows.

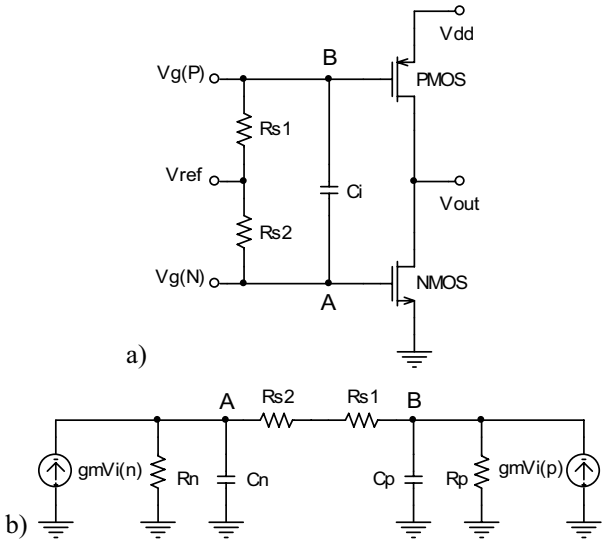

Figure 4. Class AB output stage:
a) electrical schematic;
b) small signal model

To prevent crossover distortion, output devices carry bias current. So, to prevent these distortion or large power consumption, the bias current must be controlled.
Because the preamplifier common-mode voltage is set to be a constant voltage, the gate voltage of the output transistors can be determined with the following equations [1]:

$$\begin{cases} V_{g(P)} = V_{ref} + R_{S1} I_b \\ V_{g(N)} = V_{ref} - R_{S2} I_b \end{cases} \tag{2}$$

where I_b is the bias current through the preamplifier cascode branches and $V_{g(P)}$ and $V_{g(N)}$ are the gate voltages of the PMOS and NMOS transistors, which forms the class AB output stage.

The class AB bias current can be controlled if the resistance and threshold voltage variations due to the process variations are cancelled [1].
If the gate voltages of PMOS and NMOS transistors are equal in magnitude and phase, the small voltage gain of this stage will be given by [1]:

$$A_v = \frac{V_{out}}{V_{in}} = \left(g_{m(N)} + g_{m(P)} \right) \cdot R_S \tag{3}$$

where $g_{m(N)}$ and $g_{m(P)}$ represent the output transistors transconductances and R_S is the load resistance of the line-driver.
The small signal schematic of the class AB output stage is shown in Fig. 4.b). R_N and R_P resistors represent the output resistances of nodes A and B, and C_N and C_P are the gate-source capacitors of NMOS and PMOS transistors, respectively.
In small signal, for high frequencies, the gate-source capacitors of NMOS and PMOS transistors (noted C_N and C_P, respectively) bypass R_N and R_P resistors.
If a signal is applied to the A node of the model shown in Fig. 4.b), one can write:

$$\begin{cases} v_{gN}(s) = \dfrac{I_N(s)}{sC_N} = I_P(s)\left(R_{S1} + R_{S2} \right) + \dfrac{I_P(s)}{sC_P} \\ v_{gP}(s) = \dfrac{I_P(s)}{sC_P} \end{cases} \tag{4}$$

where $v_{gN}(s)$ and $v_{gP}(s)$ are the voltages in nodes A and B and $I_N(s)$ and $I_P(s)$ represent the currents through the C_N and C_P capacitors, respectively.
By the same proceeding, if a signal is applied to the B node of the model illustrated in Fig. 4.b), finally result the following connection relations between the signal gate voltages of NMOS and PMOS transistors, which form the class AB output stage:

$$\begin{cases} v_{g(N)} = \dfrac{v_{g(P)}}{1 + \left(R_{S1} + R_{S2} \right) C_N \cdot s} \\ v_{g(P)} = \dfrac{v_{g(N)}}{1 + \left(R_{S1} + R_{S2} \right) C_P \cdot s} \end{cases} \tag{5}$$

By neglecting C_I capacitor, due to the existence of R_{S1}, R_{S2} resistors and C_N, C_P capacitors, the gate voltage of PMOS transistor differs from the

gate voltage of NMOS transistor in magnitude and phase, as equations (5) show.
Consequently, at high frequencies, the unequal driving of the output devices is the main source of distortion in the output stage [1]. To solve this problem, a relatively high C_I capacitor is used in parallel with R_{S1}/R_{S2} [1].
This capacitor bypasses R_{S1}/R_{S2} at high frequencies and causes the gate voltages of output devices to be similar in phase and magnitude. Thus, the C_I capacitor increases the linearity of the class AB stage, the main source of distortion, at high frequencies [1].
In order to choose the size of the output devices, transistors must be in saturation region even they carry the maximum current. So, the minimum aspect ratio of the output devices (for example NMOS) is equal to [1]:

$$\left(\frac{W}{L}\right)_{out} \geq \frac{2I_{out\max}}{\mu_n C_{ox}\left(V_{GS}-V_{th}\right)^2} \tag{6}$$

where V_{GS} is the gate-source voltage of output devices when carrying maximum current, V_{th} is the threshold voltage of output devices, and $I_{out\max}$ represents the maximum current of output devices.
The total currents flowing into the two transistors, which form the class AB output stage, can be written as follows:

$$\begin{cases} i_{out(N)} = I_{bias(N)} - \dfrac{v_{out(N)}}{2R_S} \\ i_{out(P)} = I_{bias(P)} + \dfrac{v_{out(P)}}{2R_S} \end{cases} \tag{7}$$

where $I_{bias(N)}$ and $I_{bias(P)}$ are the bias currents of the output devices, and $v_{out(P)} = v_{out(N)} = v_{out}$ is the output differential voltage of the class AB output stage in hypothesis that the signal voltages in the two transistors gates are identical due of the C_I capacitor's influence at high frequency. So, the total current through the single-ended load resistance of the class AB output stage can be written:

$$i_{out} = i_{out(P)} - i_{out(N)} = I_{bias(0)} + i_0 \tag{8}$$

where

$$\begin{cases} I_{bias(0)} = I_{bias(P)} - I_{bias(N)} = \dfrac{V_{com\,out}}{R_S} \\ i_0 = \dfrac{v_{out}}{R_S} \end{cases} \tag{9}$$

The maximal current through PMOS transistor results from (7), which is the sum of the bias current and half of the signal current which flows into the single-ended load resistor R_S:

$$I_{out\max(P)} = I_{bias(P)} + \frac{V_{out(P)}}{2R_S} \tag{10}$$

where $V_{out(P)}/2$ is the half of the signal voltage magnitude on the single-ended load resistance.
To obtain the minimum aspect ratio of output devices, they must be in the end of saturation region when carrying the maximum current [1]. Results:

$$V_{GS} - V_{th} = V_{DS} = V_{com\,out} - \frac{1}{2}V_{out(P)} \tag{11}$$

where V_{DS} is the drain-source voltage of output devices and $V_{com\,out}$ is the output common-mode voltage. Introducing (10) and (11) in (6), one obtains [1]:

$$\left(\frac{W}{L}\right)_{out} \geq \frac{I_{bias(P)} + \dfrac{V_{out(P)}}{2R_S}}{\dfrac{1}{2}\mu_n C_{ox}\left(V_{com\,out} - \dfrac{1}{2}\cdot V_{out(P)}\right)^2} \tag{12}$$

In order to select the optimum size, we can use two different methods [1], [8].
One of these methods consists in selecting a minimum size that causes small capacitance at the output of preamplifier. Consequently, the available bandwidth increases, but this also increases the voltage swing at nodes, especially at the gates of output devices. As consequence, the open-loop linearity is lower in this approach. But, when the feedback is applied, closed-loop linearity due to the large bandwidth is more considerable. Obviously, the advantage of this approach is that the output devices occupy small area on the chip [1].
In the second method, the output devices size is chosen larger. So, the voltage swing at nodes is reduced. Therefore, the open-loop linearity increases. Because of large parasitic capacitances at the output of preamplifier,

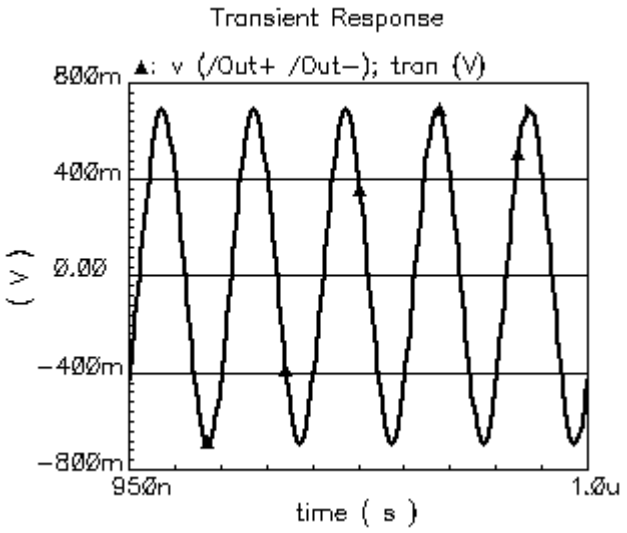

Figure 5. Differential output waveform.
($V_{in\max(diff)}$ = 380mV, f_{in}=100MHz)

associated with huge output devices, bandwidth will be decreased. A smaller bandwidth implies a reduced gain at the operating frequency and therefore a less linear closed-loop response for a given open-loop distortion level.
Results that even if this approach gives a more linear open-loop circuit, when feedback is applied a smaller linearization factor can be utilized.

The improvement of the closed-loop linearity obtained by increasing the size of the output devices is therefore less consistent than previously method. Considering this trade-off, we can find the optimum size which gives good open-loop and closed-loop linearity, by repeated simulations [1].
According to this method, the aspect ratio for NMOS and PMOS output devices are chosen 600 and 1250, respectively, smaller than other output devices of the line-drivers reported in literature. Therefore, the line-driver proposed in this paper occupies a smaller area on the chip than others presented in literature.
As we previously mentioned, C_I is used to make the gate voltages of NMOS and PMOS transistors equal at high frequencies. So, C_I increases the linearity for both methods previously presented. In the following simulations we consider C_I = **10pF**.

4. Simulations results

The voltage supply of the proposed line-driver is 1.5V and drives a 75 Ω resistive load and 10 pF single-ended capacitors. The line driver power consumption is 46mW.
Fig. 5 shows a output waveform of the line driver when the differential input signal (having $V_{in\max(diff)}$=**380mV** magnitude and f_{in}=**100MHz** frequency) is applied. The differential output signal has about 1.4V (peak to peak) value.

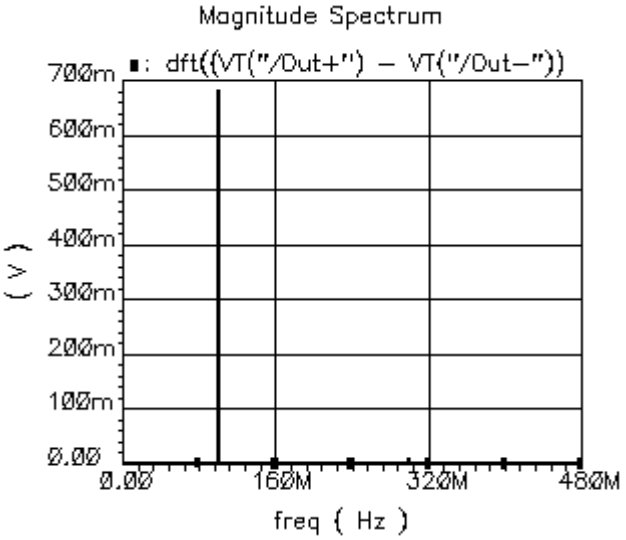

Figure 6. Spectrum of the differential output signal.
($V_{in\max(diff)}$ = 380mV, f_{in}=100MHz)

Magnitude spectrum of this signal is shown in Figure 6. It shows a very small distortion of the line driver differential output signal.

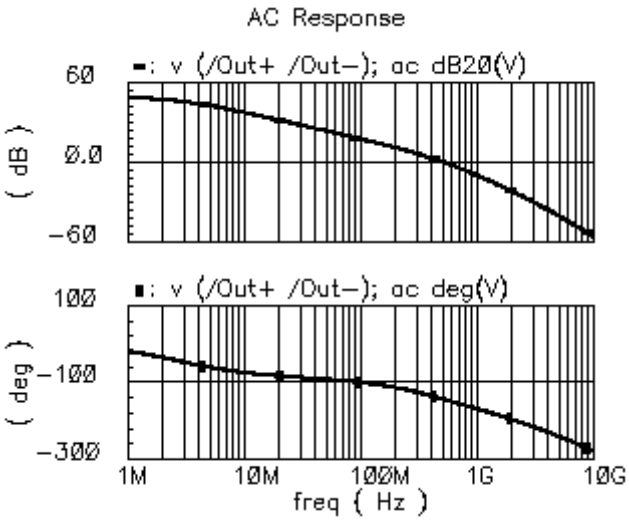

Figure 7. Open-loop Bode characteristics of the line driver.

The open-loop and closed-loop frequency response of the line-driver while driving a **75 Ω** and **10pF** single-ended output capacitors are shown in Fig. 7 and Fig. 8, respectively.
Fig. 7 shows a unity frequency of 500MHz and phase margin of 40°.
Fig. 8 shows -3dB bandwidth of **345MHz** (better than others line drivers reported in literature) with phase margin of **60°**, which assure a good stability of the closed-loop circuit.

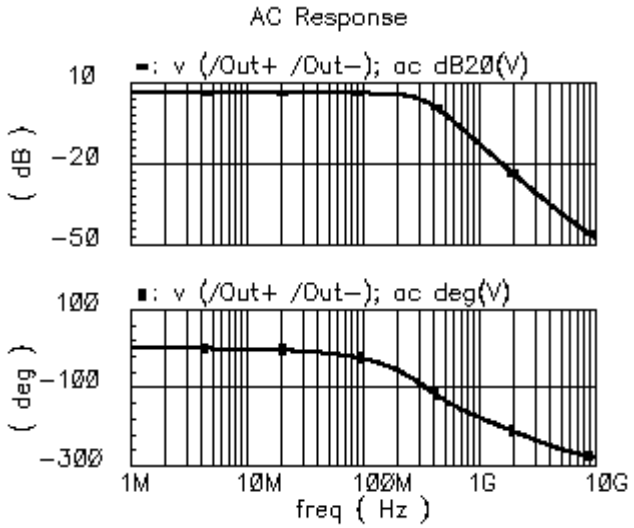

Figure 8. Closed-loop Bode characteristics of the line driver.

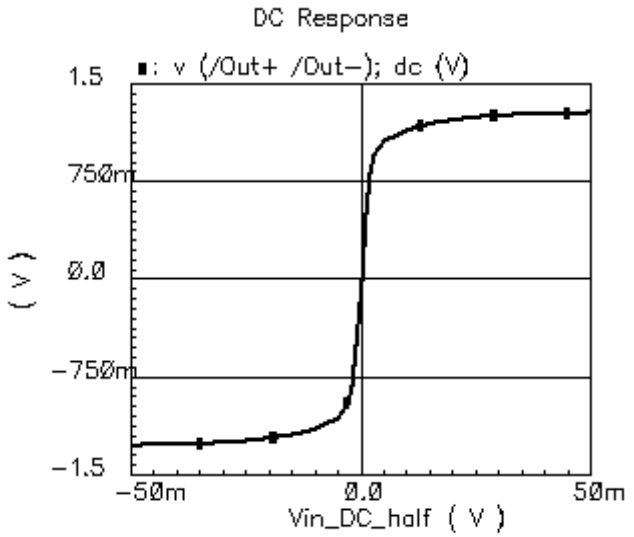

Figure 9. Open-loop dc characteristic of the line driver.

In Fig. 9 the open-loop d.c. characteristics of the proposed line-driver is shown. Comparatively, in Fig. 10 the closed-loop d.c. characteristic of the line driver is presented.

So, one can observe a significant increase of the closed-loop linearity of the proposed line-driver.

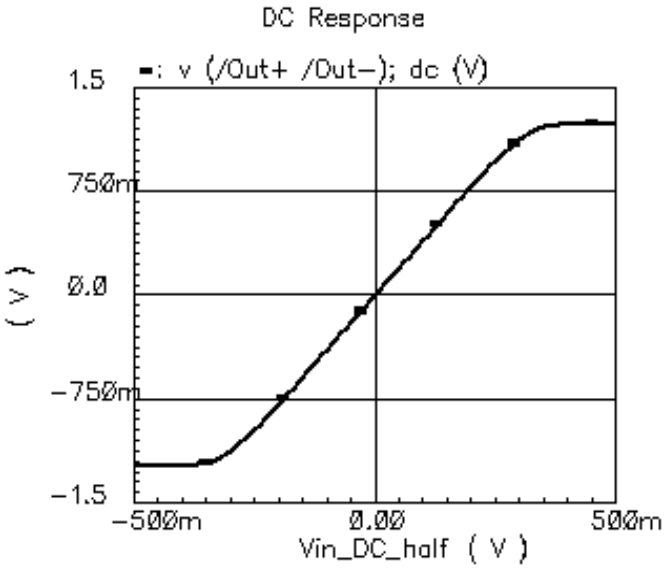

Figure 10. Closed-loop dc characteristic of the line driver.

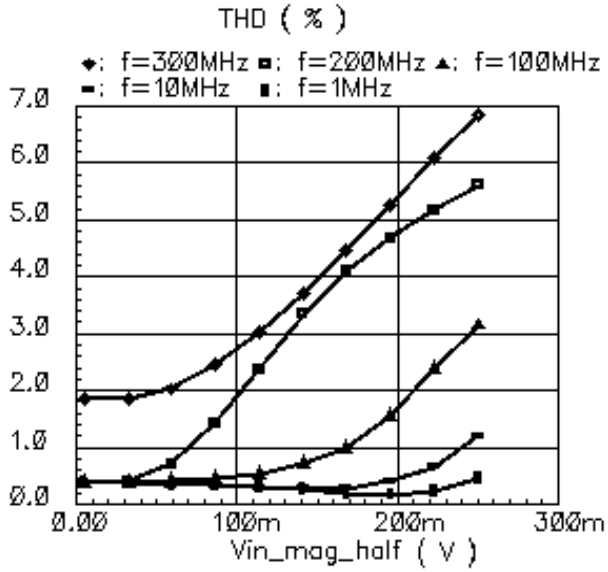

Figure 11. ***THD*** **value of differential output signal.** (**$V_{in\max(diff)}$ = 10mV – 500mV**; **f_{in}=1MHz, 10MHz, 100MHz, 200MHz, 300MHz**)

To asses the small and large signal linearity for the proposed line-driver, the ***THD*** of the output differential voltage is calculated. So, in Fig. 11, the ***THD*** value of the output differential voltage depending on input signal magnitude for different values of frequency is shown ($V_{in\max(diff)}$**=10mV–500mV**, f_{in}**=1MHz**, **10MHz**, **100MHz**, **200MHz**, **300MHz**).
One can observe from Fig. 11 a good linearity of the proposed circuit, even for high frequencies.

5. Concluding remarks

In this paper a new low voltage, fully differential line-driver, which provides a good linearity, a performing frequency response and low power consumption, is presented. The line-driver drives a 75Ω resistive load and 10 pF single-ended capacitors.
By using a differential architecture for the proposed circuit gives an important decrease of the common-mode perturbations, such as the substrate noise or the power supply noise, and also the even order harmonics cancel.
The proposed circuit is formed of two stages, an input folded cascode preamplifier built by an input differential pair with NMOS transistors, and also a class AB output stage. The line-driver uses two separate common-mode feedback circuits, which determines a significant decrease of distortions.
The simulations made in 0.13 μm CMOS process confirm the theoretically obtained results.

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