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# IMPROVED ENCODER CIRCUIT FOR INVERSE DIFFERENTIAL MANCHESTER CODE

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***Abstract.*** *An improved encoder circuit that operates at any frequency is presented. As no one shot circuits are used, its operation is extended to higher values of the frequency, as compared with a previous approach [1].This results in improved reliability of the circuit operation.*

***Keywords:*** *Line Code, inverse differential Manchester, encoder circuit, practical implementation.*

## Introduction

The inverse differential Manchester code was introduced in [1]. The differential Manchester code is used in a number of communication and electronic systems and it was adopted by IEEE to be used in the physical layer in Token Ring Local Area Networks [2].

Its coding rules are: there is always a transition at the middle of the encoded bit and an extra transition is added at the beginning of the bit interval when sending a '1'. No extra transition is added for '0'.

The inverse differential Manchester encoder circuit presented in [1] shows several drawbacks:

1. It uses two one shot circuits. These are known for their not so famous reliability in a repetitive mode of operation.

2. The factor that limits the high-frequency operation is the one shot circuit. For instance, a JK flip-flop such as 7473 from the TTL logic circuit family used to build the encoder is known to have a maximum clock frequency of 15 MHz. The author reported a maximum usable clock frequency for the encoder circuit of 95,21 kHz, as he chose the output pulse duration of the one shots to be 5 $\mu s$ .

3. The assumption made in the formula giving the maximum operating frequency $f_{\max} = 1/[8(t_r + t_f) + 2\tau]$, namely that $\tau$ is made very small and can be neglected with respect to $8(t_r + t_f)$ is not a valid one, since the time constant of the one shot can not be made

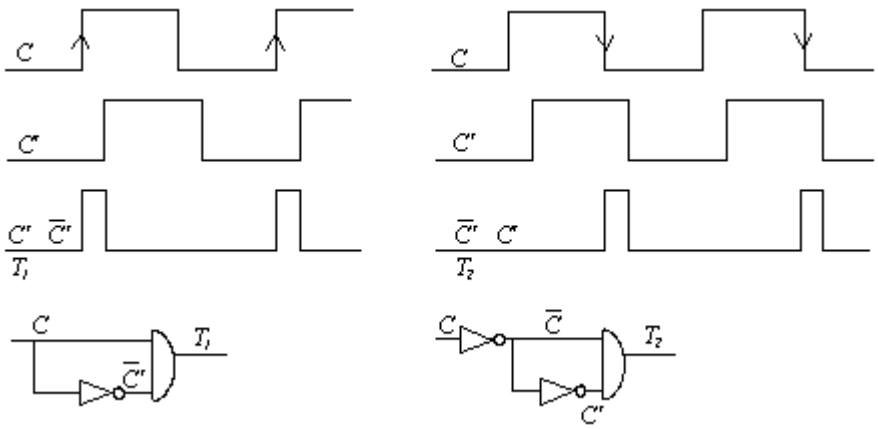


**Figure 1. Edge detection circuits.**

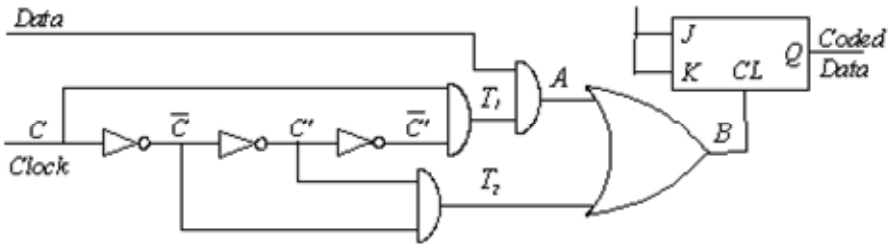


**Figure 2. Improved encoder circuit.**

arbitrarily small.

## Encoder design

Since the one shots are used to detect clock transitions, they can be replaced by the simple edge detection circuits [7], [8], represented in Fig. 1.

Here c' is a delayed version of the clock signal c.

Obviously,

$$T1 = c \cdot \overline{c}' \qquad T2 = \overline{c} \cdot c' \tag{1}$$

where " . " denotes the logical AND operation and the over bar denotes the logical inverse operation.

Then, the schematic of the multipurpose encoder as proposed in [1] can be simplified as shown in Fig. 2.

$$A = T_1 \cdot Data \tag{2}$$

$$B = A \cup T_2 \tag{3}$$

where "$\cup$" denotes logical OR operation

Replacing the OR gate by a NAND gate with inverted inputs, according to de Morgan's theorems, the schematic in Fig.3 results, which is a more practical implementation of the encoder circuit.

The operation of the encoder circuit is illustrated by the timing diagrams in Fig.4.

## Conclusions

An improved encoder circuit as compared with that introduced in [1] was synthesized. Its frequency of operation is limited by the limit frequency achieved by the present CMOS technology. Its schematic is quite simple and does not involve one shot circuits.

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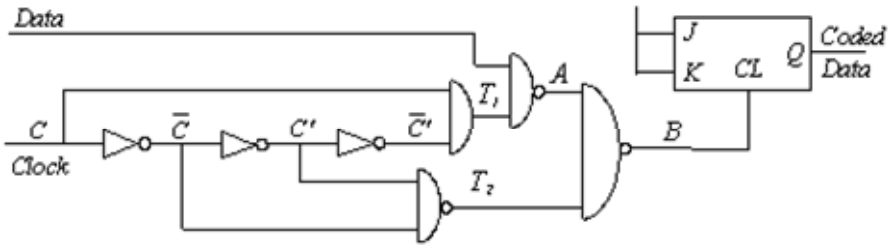


**Figure 3. Practical implementation.**

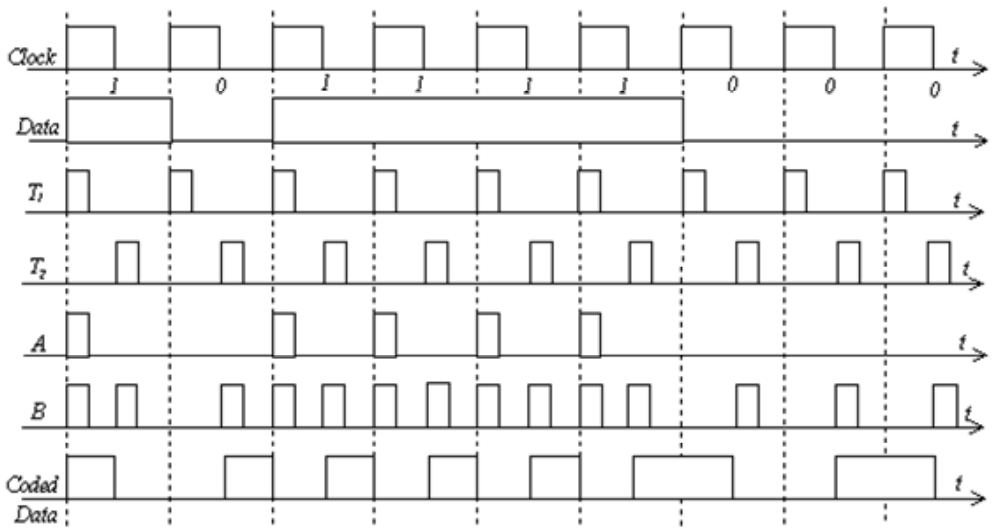


**Figure 4. Waveforms illustrating the operation of the encoder circuit.**

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