8th International Conference on DEVELOPMENT AND APPLICATION SYSTEMS
Suceava, Romania, May 25 – 27, 2006

DEVELOPMENT OF A UNIVERSAL HARDWARE PLATFORM FOR WIRELESS COMMUNICATION

Luc DE BACKER, Lieven DE STRYCKER, Jean-Pierre GOEMAERE, Koen VANDECASTEELE, Wim VAN HOUCKE
"KaHo Sint-Lieven" Technical University
Gebroeders Desmetstraat nr. 1, B-9000 Gent
dramco@kahosl.be

Abstract. *As Wireless Personal Area Network (WPAN) standards, such as Bluetooth, Zigbee, RFID become more common, it might be interesting to improve the functionality of existing products by adding a wireless interface. To test the possibilities and limitations of the different standards, a universal hardware platform which supports different wireless standards is a handy tool. In this work a hardware platform that allows rapid prototyping and fast evaluation is described. The platform allows implementing both the functionality of the existing product and the wireless standard of interest. For the implementation of the standardized wireless interface, RF extension boards are plugged onto the universal hardware platform and the required software libraries are provided.*
Keywords*: development platform, WPAN, microcontroller, FPGA.*

Introduction

As a wide variety of standards for wireless communication exist, each working in their own proper way, research is needed to find the most appropriate standard for the desired embedded application. The use of a standard depends on the requirements of the application (such as desired network topology, expected data rate, range, etc). Small and mid-sized companies often do neither have the financial reserves nor the staff to perform this research. In Belgium, this research can be done in collaboration with other companies and a (technical) university. This co-operation gives the companies the opportunity to get access to scientific knowledge and expertise in this field.

DraMCo Research, which is a part of the electronic department of KaHo Technical University, is specialized in digital wireless communication. DraMCo engaged itself together with more than ten companies, to investigate the possibilities of the low power, low rate and short distance wireless communication standards [1] [2]. By studying and performing tests on e.g. Bluetooth, RFID and Zigbee, DraMCo offers an in-depth view of the technology and the possibilities of these standards [6] [7] [8] [9]. As a part of the research project, a hardware platform and accompanying software, implementing basic functionality of the above specified standards are developed. Hereby, the companies have a platform that offers them the possibility to evaluate a standard for a first prototype in a time-efficient way.

In the remaining of this document the requirements, the hardware components and the layout of the platform are discussed in depth. Afterwards, the functionality of the resulting hardware platform is evaluated.

Requirements of the platform

As described above, the goal is to offer a platform that can be used for rapid prototyping. As rapid prototyping stands for easy and fast implementation, programming and testing of the global functionality, it does not intend to implement all the final features in a cost and silicon efficient way [3] [4] [5].

The selection of the hardware components and software utilities are influenced by the mentioned key requirements. These can be translated into the following claims:

- Limit the costs of use and development of the platform. Multiple vendors offer free samples and various programming tools are distributed under a free-to-use license.
- Whenever possible, use the same components and software as is used in the companies. This reduces their time for assimilation.
- Offer a wide and clear tutorial. This limits the required time for learning the board.

When taking these claims into account, the use of the platform in an industrial testing environment is more likely.

As a wide variety of radios and antennas can be purchased from various manufacturers, the project did not intend to develop these modules. However, interfaces to existing RF modules are crucial elements on the platform.

Figure 1 gives a schematic overview of the foreseen functionality of the platform (grey). As can be seen, interfacing to RF modules for data exchange, to a computer for debugging, etc. are important elements.

Hardware components

Figure 2 shows the designed platform which has the following major components:

- Atmel AtMega128L microcontroller [10].
- Xilinx Spartan II 150 FPGA [11].
- Two 50 pin GPIO busses, two RS232 connectors.
- Cypress CY7C1069AV33 2 Mbyte SRAM.

The microcontroller can be seen as the actual "heart" of the final product. The intended functionality is programmed into this chip, i.e. the wireless communication protocol shall be on this module. The AtMega is an easy to use microcontroller. It has 128Kbytes of flash, 4 Kbytes of EEPROM and 4 Kbytes of RAM memory and offer up to six 8-bit ports with multiple functionalities (ADC, JTAG, etc.). Most of the instructions are one cycle commands. The chip is in-system programmable (ISP) and can also be programmed with the JTAG interface. As it is to be used in battery powered wireless communication systems, the 3.3 V version of the chip is chosen. This limits the clock to only 8 MHz. Various white papers, tutorials, free programming and debugging tools can be found [10] [13].

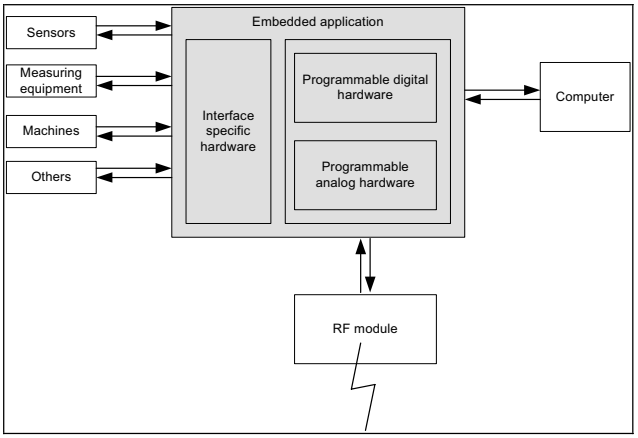

Figure 1. Schematic overview of the platform.

For interfacing with the RF modules, for debugging, … two RS232 connectors and two 50 pin general purpose input/output (GPIO) busses are foreseen. For serial communication an additional chip is needed to transform the I/O to the appropriate signal levels [14]. One of the GPIO busses (GPIO bus 1) is only connected to the FPGA. The other (GPIO bus 2) outputs all the data pins of the microcontroller.

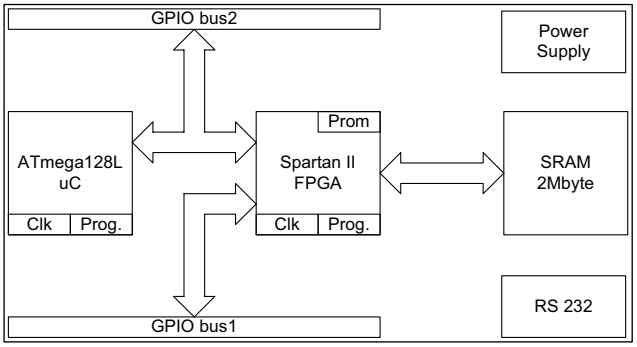

Figure 2. Schematic overview of the hardware.

The FPGA can be seen as the co-processor and is connected to the GPIO busses and the memory module. GPIO bus 2, which outputs the data pins of the microcontroller, is also connected to the FPGA. Hence, the FPGA

reduces the workload of the microcontroller (for example for time critical tasks, such as video signals to an LCD screen). GPIO bus 1 can dynamically be modified via the chip to output requested data. In combination with the memory chip, the FPGA offers the possibility to log information in a non-volatile way. The FPGA configuration file needs to be loaded at any start-up of the chip. This can be done directly into the FPGA via a PC or by a PROM module available on the board. In the latter case the configuration file is primary loaded to the PROM. Programming the FGPA or PROM can be done with free software, using VHDL and the JTAG interface. The FPGA needs a power supply of 3.3 V and 2.5 V.

As memory module, a 2 Mbyte SRAM chip has been chosen [12]. It can be accessed through the FPGA. The module is a high-speed (an access time of 12 ns) CMOS Static RAM module, operating at 3.3 V. The use of SRAM implies that no refresh of its data needs to be organized.

Layout

The platform is realised as a six-layered board (figure 3). This has been chosen to minimize the physical size and to reduce interference of adjacent signals.

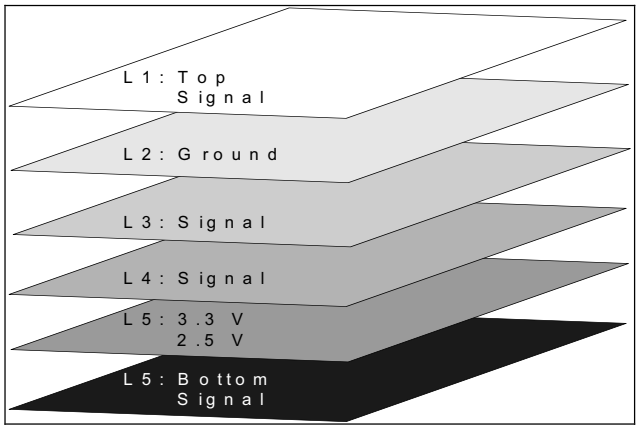

Figure 3. Overview of the different layers.

The top and bottom layers contain the hardware components. The second layer is a ground layer and the fifth is the power supply layer. The latter is mainly a 3.3 V surface power supply, but also 2.5 V (to the FPGA) is on this layer.
It is worth mentioning that at every power supply connection of a chip a decoupling capacitor is placed to reduce current fluctuations on the power supply layer.

Result and possible improvements

The hardware platform has successfully been tested to run Bluetooth, Zigbee and RFID. Even an implementation of RFID together with Zigbee gave satisfying results.

The use of the high speed static RAM with its high capacity of 2 Mbytes as memory module, offers great possibilities and requires no driver for refreshing its data. However, the use of SRAM increases the cost of the board significantly. Here, a trade-off between price and program simplicity needs to be made.

Conclusion

As an aid to small and mid-sized companies interested in the new possibilities of low power, low data rate, short distance wireless communication, a hardware platform has been developed (figure 4).

By taking into account the knowledge of hardware in the companies when developing the board, the step to use this platform is reduced. A universal hardware platform offers the opportunities that only one hardware platform has to be studied (instead of getting to know all platforms for every module of interest) and only one programming, compiling and debugging environment needs to be known.

Its functionality has extensively been tested and concluded into positive results.

As rapid prototyping platform it has been offered to students of the technical university to realize their final project and in a short period a working device has been developed, even for topics different from wireless communication.

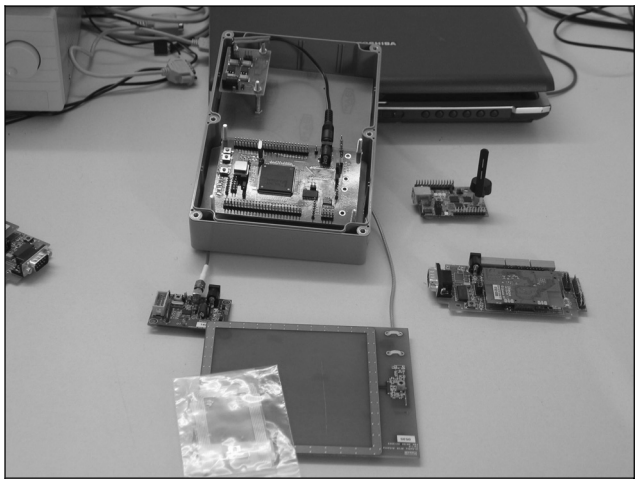

Figure 4. Universal hardware platform with its RF modules for Bluetooth, RFID and Zigbee.

So, next to its rapid prototyping functionality for wireless communication standards it can be used for a wide variety of applications.

References

[1] De Backer, Luc, De Strycker, Lieven, Goemaere, Jean-Pierre, Vandecasteele Koen, Van Houcke, Wim (2005) *Design and Evaluation of a Digital Wireless Development Platform*, Vol. 2, ICMCS-05.

[2] http://ingenieur.kahosl.be/projecten/iwt_elektronica

[3] P. Papazian, M. Babait a, A. Popovici, A. Avram, I. Lie (2005) *Signal Generating Techniques Using PIC16F84 Microcontrollers*, Vol. 2, ICMCS-05.

[4] http://www.freeio.org

[5] http://www.openhardware.net

[6] http://www.ieee802.org

[7] http://www.bluetooth.org

[8] http://www.zigbee.org

[9] http://www.wg8.de

[10] http://www.atmel.com

[11] http://www.xilinx.com

[12] http://www.cypress.com

[13] http://www.avrfreaks.com

[14] http://www.maxim-ic.com

Acknowledgement

The realisation of this hardware platform and this paper are part of the EPANuS project “Research and Development on Embedded Personal Area Networks using Standards”, (TETRA project n° 40239), supported by the Flemish government, IWT.