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NEW CONCEPTS IN COMBINATIONAL CIRCUIT DESIGN FOR TESTABILITY

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Abstract. *Permanent amelioration of the numeric equipment's performances comes with an increase in the complexity of the digital structures that are designed, which makes it difficult, some times up to impossible, to test them. This can lead to an impossibility of creating complex digital equipment. .This paper proposes new concepts of design for testability (DFT) based on reconfiguring and homogenizing the digital structures during the tests by using complementary reconfigurable elementary digital structures (CREDS) and elementary structures that change the parity of the digital signal (ESCP). Homogenizing the structure during the testing allows us to obtain a plenitude of universal and minimal control/diagnostics tests. The results can serve as a basis when designing for testability arbitrary combinational circuits with multiple entry points.*

Introduction

Traditional methods used in the design for testability of digital structures are based on auxiliary concepts that aim to improve controllability (C) and observation (O) as a result of using logics and auxiliary pins, structural, functional or logic properties or special methods which target only specific structures or logic elements. Each design for testability improvement usually makes the design and fabrication process more complex, requires extra surface (or volume) on the crystal as consequence of the extra connection points and auxiliary logic which are included to make testability better. Unfortunately, the results obtained when putting the basis for the CC testability concepts did not leave up to the expectations. The increased number of auxiliary connection points has a negative effect on the chip's technology, and the excessive increase of logic levels leads to grave performance losses of the designed equipment.

Basic notions and definitions

This paper is based on notions such as: the extraordinary set of binary signals of a stimulus array, extraordinary or dominant value of the binary signal, regularization procedure, regular and partially regular structure [1], reconfigurable digital structure (REDS) complementary REDS [2], dual REDS [3], elementary structure that changes the binary signal parity (ESCP) [4], homogenization of the digital structure to check or diagnose, tests with a minimum number of stimulus arrays and universal tests [5].

Between the various types of logic gates there are a number of relations. Two logic gates with the same number of input points whose truth table coincide are called equivalent. The signification of equivalent gates is that they allow replacing one gate in the circuit with its equivalent without changing the circuit's logic function.

Two logic gates with the same number of input points are named duals is for any set of values for the input signals, the values of the output signals are in opposition. It can be easily observed that adding or removing an inverter at the output of one gate in the dual pair changes the relations between these gates' properties switching from equivalence to duality and the opposite.

If the binary values of a set coincide, then the set is homogenous. For example, the sets 000 and 111 are homogenous. The sets 001 and 101 are not homogenous.

Two logic gates with the same number of input points are called complementary if the output signals are opposite for any non homogenous binary signal applied on the inputs.

During the design phase, various circuit parts that are built from a single type of logic gates – AND or OR – can be highlighted. These

portions of a circuit that are made up from a single type of logic gates – AND or OR are called maximally degenerated circuits. A sub-circuit or a maximally degenerated circuit is equivalent with a logic gate made of the respective type and with the same number of input points. Therefore, the regulation procedure allows highlighting the degree of homogeneity of the structure that is being analyzed, and the non-homogeneous gates show what has to be changed in order to enhance the controllability and stability parameters. Adding a reverser on the output connection of the maximally degenerated circuit is equivalent with adding a reverser on the output connexion of the logic gates of the same type.
The meaning of a digital structure's homogeneity lies, in fact, in decreasing the minimal number of stimulus arrays used to diagnose towards the number of stimulus arrays needed to diagnose a logic gate with n input points:

$$T = n \tag{1}$$

Other notions and definitions needed to fully comprehend this paper can found in [6].

The problem

Consider the Boolean function, defined through the Karnaugh diagram (table 1), in figure 1:

Karnaugh diagram

Table 1

de \ abc	000	001	011	010	110	111	101	100
00						1		
01						1		
11	1	1	1	1	1	1	1	1
10						1		

de abc

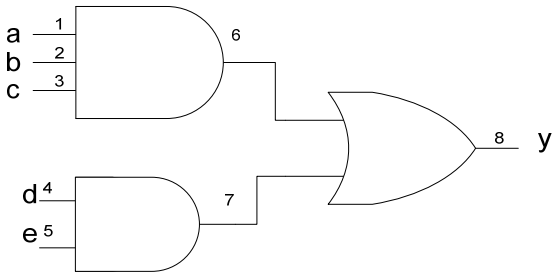

Figure 1. Logic circuit without redundancy.

According to the maximal coverage of the Boolean function principle we can obtain the minimal and without redundancy form:

$$y = abc \vee de \tag{2}$$

Within the general concept of design for testability, the specific problem of creating the different design and testing concept of CC without fan-outs in simple Boolean base and CREDS, and obtaining a universal and minimal unit of checking / diagnose tests arises. As a basic procedure used to solve the problem, reconfiguring the circuit in testing mode is used. The aim is to obtain homogeneity of the logic structure.

Design for testability concepts in simple Boolean base for combinational circuits without fan-outs

A logic circuit can be created in simple Boolean base (AND, OR, NOT), in universal mono-functional base (AND-NOT or OR-NOT), in complex base, etc. The diversity of logic gates for the tested structure implies diversity in the elaboration of the concepts used to ensure homogeneity. The concepts are based – in general, on using REDS and ESCP, analysis and/or structural algorithms, but on heuristics and intuitive procedures as well.

Obtaining circuit homogeneity by using CREDS with 2 command signals

Creating a circuit in CREDS base implies using the algorithm presented in [2], meaning the replacement of each gate in the circuit presented in figure 1 with the respective CREDS structure.

This way the circuit in figure 2,a is obtained, which, when using the command signals C1=1 and C2=0 will be reconfigured in normal operating mode (fig. 2,b).
In testing mode 1 (fig. 2,c), the structure is reconfigured and we obtain the maximally degenerated AND circuit. The circuit is functionally equivalent to the AND gate with the same number of inputs. When C_1=0 and C_2=0, the circuit will be reconfigured in testing mode 2 for the maximally degenerated OR structure, functionally equivalent to the AND gate with the same number of inputs.

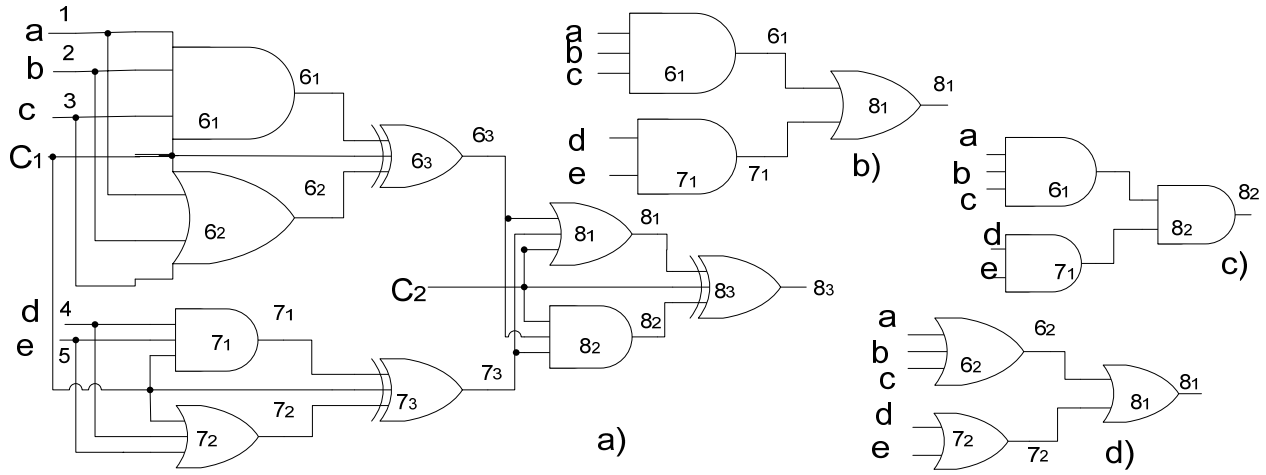

Figure 2. Homogenisation in CREDS base with 2 command signals: a) circuit designed for testability in a CREDS base ; b) equivalent circuit in normal functioning mode; c) AND maximally degenerated structure; d) OR maximally degenerated structure.

For the DFT in CREDS base, the T_c control test for absence of defects on the primary inputs of the circuit in figure 2, a will contain the extraordinary test 11111 of the AND gate and the 00000 extraordinary test of the OR gate:

$$T_c = \{11111, 00000\} \quad (3)$$

The diagnosis test for the basic gates of the SDERC will contain the stimulus arrays:

$$T_{d\&}=\{01111,10111,11011, 11101,11110 \quad (4)$$

The diagnosis test for the defects of "shadow" gates in CREDS will contain the stimulus arrays:

$$T_{d\vee}=\{10000,01000,00100,00010,00001\} \quad (5)$$

Obtaining homogeneity for a circuit using a command signal and a ESCP

This solution differs from the previous in that it uses only one command signal, a delay element for the command signal C1, applied at the CREDS inputs for the second level (fig.3). When C1=1 and C'1=1, ESCP will operate as a reverser and, so, the circuit will be reconfigured in mode 1 of testing the maximally degenerate AND structure equivalent with an AND gate with the same number of inputs. Finally, when C1=0 and C'1=0, the circuit will be reconfigured in testing mode 2 of the maximally degenerated OR structure, functionally equivalent with an AND gate with the same number of inputs.

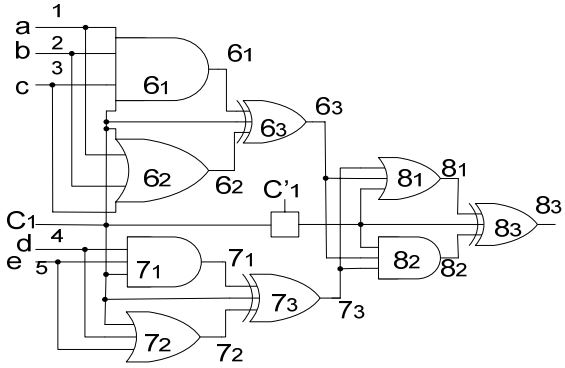

Figure 3. Homogeneity concepts based on using a single command signal and a ESCP

Regarding the Tc control tests, the Td diagnosis tests and the number and components of the

stimulus array unit, the results are the same as in previous case**.** The advantage lies in the possibility to decrease the number of auxiliary connection points by using a ESCP command signal coder.

Increasing controllability and homogeneity based on using a single CREDS

Because the controllability of gate 8, placed on level II of the circuit in figure ` is much smaller than the IP controllability, we will replace gate 8 with the respective CREDS (fig. 4).
In practice, most often a less rigorous diagnosis is enough, diagnosis method that can be obtained with less means. In figure 4, such a solution is suggested, which is based on using a single CREDS to ensure normal operating mode (C_1=0) and testing mode 1 (C_1=1), where the circuit homogeneity will be performed in an AND gate.

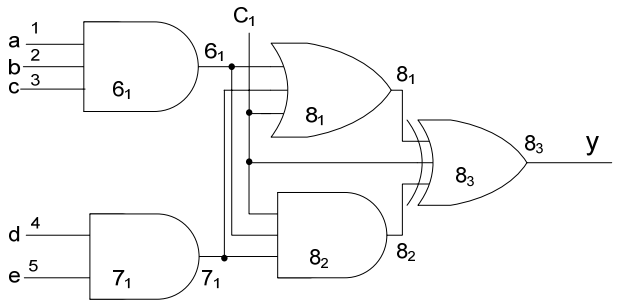

Figure 4. Circuit homogeneity based on using a single CREDS

Circuit configurations in these modes with the respective configurations in figures 2,b and 2,c. The T_4 diagnosis test contains the same stimulus arrays in field of "1" ("0" on the diagonal), which were obtained previously. However, this test also has weak points, as the inputs for the OR gate 8_1 were left without diagnostic. In order to perform a diagnosis for the ≡ 0, ≡ 1 defects at the 8_1 gate's inputs, applying three auxiliary stimulus arrays is needed, arrays which ensure the 00,01 and 10 combinations. Because only the resulting AND gate is diagnosed in testing mode 1, the three auxiliary stimulus arrays must be used when cost restrictions are imposed.

Conclusions

The proposed concepts for design for testability reflect a new vision on functional, structural and logic correlations of circuits under construction and allow using circuit homogeneity to obtain universal and minimal control and diagnosis tests. Test universality, in the end, could lead to a single unit of diagnosis tests for a digital structure with a given topology and the same number of inputs.

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