DFT: CONCEIVING DIAGNOSIS TESTS FOR RECONFIGURABLE REPETITIVE COMBINATIONAL CIRCUITS

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Abstract. *Minimizing the number of control/diagnosis tests for a combinational circuit can be achieved, in some cases through regularization – replacing some of the circuit's logic gates with equivalent gates in such a manner as to have most of the circuit represented by gates of the same type – AND or OR. This homogeneous partition can be replaced by a logic gate of the same type and with the same number of inputs which allows diagnosing the partition defects with a minimal number of stimulus arrays. This older idea, in the light of design for testability in reconfigurable elementary digital structures base leads to the complete circuit homogeneity as a true possibility. As such, conceiving procedures to synthesize the universal diagnosis test in the design phase becomes more important. This would simplify the way tests are ran and how they are run and it would lead to improving ….*
Keywords: *repetitive circuit, reconfigurable, complementary, parity, universal test unit, diagnosis.*

Introduction

Within the design for testability of combinational circuits based on the use of reconfigurable elementary digital structures (REDS) and elementary parity changing structures (EPCS), the homogeneity concept assumes a specific approach to the procedure of conceiving the control and diagnosis tests in order to obtain a minimal and universal stimulus array unit. In principle, within the homogeneity result we can obtain maximally degenerated structures, functionally equivalent with the AND or OR logic gates. From the organization principle of the positive logic and the negative logic it becomes clear that the control / diagnosis test unit for the AND gate can be obtained from the test unit of the OR gate and the opposite. On the other hand, the AND-NOT or OR-NOT homogeneous structures with a even number of levels lead, in the event of homogenization to the same AND or OR structure with unchanged topology. The initial digital structures with an odd number of levels, created in simple Boolean base lead to the creation of functionally equivalent circuits with the same basic topology in AND-NOT or OR-NOT base, but with an extra reverser on the primary output connection. In testing mode, the structures created in CREDS base will be configured as such so that the levels containing AND-NOT or OR-NOT gates will alternate within the circuit, which will lead in the end to the same equivalent AND or OR gates with the same number of inputs. In general, because reconfiguring the circuit already conceived when designing for testability in CREDS base leads to an equivalent AND or OR gate, the origin or the minimal and universal control / diagnosis number of tests becomes clear.
Repetitive circuits, unlike the non repetitive digital structures, contain fan-outs, convergence points of the primary inputs (PI). In general, each fan-out, no matter the equal or opposite parity of the convergent signals requires an extra stimulus array. This paper presents concepts used to conceive the minimal and universal control / diagnosis tests in the design for testability context for digital circuits in CREDS and EPCS base, while considering a way to maintain a high technologic factor by using a minimal number of auxiliary connection points.

Basic notions and definitions

This paper is based on the notions of extraordinary binary signal values, extraordinary or dominant logic value of the binary signal, regulation procedure, regular and partially regular structure, reconfigurable elementary

digital structure (REDS, complementary REDS (CREDS) [2], dual REDS (DREDS) [3], elementary structure that changes the binary signal parity (ESCP) [4], homogeneity of the digital structure to check / diagnose, minimal number of stimulus array test unit and universal tests [5].

A dominant (blocking) logic value of a binary signal at a gate's input is the logic value of the signal which, applied on one input determines in an equivoque manner the output logic value. For example, the logic signal "0" applied on the input of a AND (AND-NOT) gate equivocally determines the "0" ("1") signal at the gate's output.

The logic value at the gate output which is different of all other gate reactions is called an extraordinary reaction.

The unit, the binary values of the stimulus array for which an extraordinary reaction appears is called an extraordinary unit.

An extraordinary logic value of the binary signal at a gate's input is the value that the signal has in the extraordinary unit. For example, "1" is the value of the extraordinary reaction for an AND gate. "1" is also the extraordinary logic value of the gate's input signal. The meaning of an extraordinary unit lies in the possibility of detecting all ≡0 or ≡1 defects at the gate inputs.

Other notions and definitions can be found in [6].

The problem

Structural particularities of CC with convergent fan-outs in the primary inputs leaves a mark on the way control and diagnosis tests are created. The problem of conceiving a method of synthesis for the control and diagnostic tests for CC with convergent signals that have equal and opposite fan-out parities exists.

Conceiving universal and minimal tests to diagnose CC with convergent signals for the primary input fan-outs

A repetitive combinational circuit (CC) represents a digital structure with convergent signals for the primary input fan-outs. Combinational circuits, according to the number of reversers on the signal's propagation paths can be: a) with equal parity; b) with diverse parity. Because the synthesis methods for these two types of CC each have specific properties, caused amongst other by the design in CREDS and EPCS base, the generation of test units for both categories will be presented separately. This is also imposed by the necessity of obtaining universal and minimal tests to diagnose constant singular defects (DC).

Characteristics of universal and minimal control / diagnostics test synthesis for CC with equal convergent signal parity for the primary input fan-outs.

Having fan-outs in the circuit affects both the extraordinary unit (stimulus array), and some stimulus arrays in the universal test. We can differentiate 2 situations for the fan-out signal parity correlations: a) equal parity; b) opposite parity.

Universal test synthesis for CC with equal parity

Consider the non redundant Boolean function y_e represented in the Karnaugh diagram (table 1):

$$y_e = a \cdot b \cdot c \vee c \cdot d \cdot e \qquad (1)$$

Following the synthesis in simple Boolean base we get a repetitive CC with equal parity for the convergent fan-out signals (fig. 1,a). Even a superficial analysis on whether we can generate an universal and minimal diagnosis test would reveal that when applying the extraordinary stimulus array, the values of the signals on the c1 and c2 connections are identical, and, therefore no logical contradictions can appear, while in the universal test signal mixtures of 01 and 10 must appear on the c^1 and c^2 connections. This does not happen in this case. It figures that in order to

Karnaugh diagram

Table 1

abc / de	000	001	011	010	110	111	101	100
00						1		
01						1		
11		1	1			1	1	
10						1		

cde abc

Tests of equivalent gate AND

Table 2

No. test	Binary signals a	b	c^1	c^2	d	e	y_{pe}	Activation ESCP in testing mode 1
1	0	1	1	1	1	1	0	$C'_1=0$
2	1	0	1	1	1	1	0	$C'_1=0$
3	1	1	0	1	1	1	0	$C'_1=1$
4	1	1	1	0	1	1	0	$C'_1=1$
5	1	1	1	1	0	1	0	$C'_1=0$
6	1	1	1	1	1	0	0	$C'_1=0$

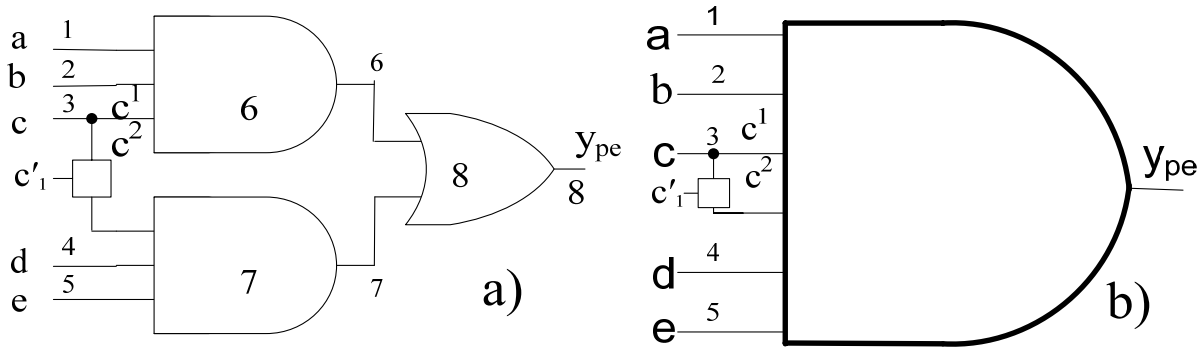


Figure 1. CC with re-convergent fan-out with equal signal parity (a), equivalent AND gate with fan-out and equal parities in testing mode 1 (b).

transform the test into an universal one for the c^2 connection, installing a ESCP is needed. During the design for testability phase, each of the 6,7 and 8 gates are replaced with the respective CREDS and we get a digital structure whose description in normal functioning mode will be:

$$y=((C_1 abc^1 \oplus C_1 \oplus (C_1 \vee a \vee b \vee c^1)) \vee (c_1^1 \oplus c^2) de C_1 \oplus C_1 \oplus (C_1 \vee d \vee e \vee (c_1^1 \oplus c^2)) \vee C_2)_{|C_1=1,\, c_1^1=0,\, C_2=0} \quad , \qquad (2)$$

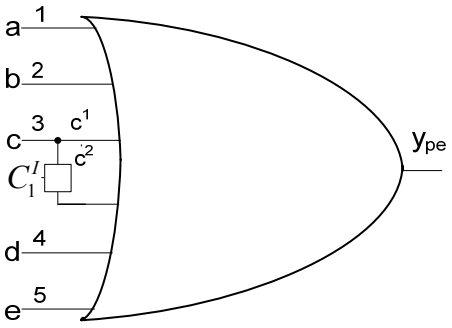
In testing mode 1 (C_1=1 and C_2 =1), the digital structure created in CREDS base is described by the Boolean function:

$$y=((C_1 abc^1 \oplus C_1 \oplus (C_1 \vee a \vee b \vee c^1)) \& (c_1^1 \oplus c^2) de C_1 \oplus C_1 \oplus (C_1 \vee d \vee e \vee (c_1^1 \oplus c^2)) \& C_2)_{|C_1=1,\, c_1^1=0,\, C_2=1} \quad , \qquad (3)$$

Except for the case when, artificially, in order to ensure the universality of the test and the result of opposite values for the c1 and c2 signals we need to activate the ESCP, meaning C'=1.

In testing mode 2 (C_1=0 and C_2=0) the digital structure created in CREDS base is described by the Boolean function:

$$y=((C_1 ab\bar{c}\oplus C_1\oplus(C_1\vee a\vee b\vee c^1))\vee((c_1^1\oplus c^2)\cdot C_1 de\oplus C_1\oplus((c_1^1\oplus c^2)\vee C_1\vee d\vee e))$$
$$\vee C_2)_{|C_1=0,C_2=0,c_1^1=0}\quad , \tag{4}$$



Tests of equivalent gate OR Table 3

No. test	Binary signals a b c^1 c^2 d e y_{pe}	Activation ESCP in testing mode 1
1	1 0 0 0 0 0 1	C'_1=0
2	0 1 0 0 0 0 1	C'_1=0
3	0 0 1 0 0 0 1	C'_1=1
4	0 0 0 1 0 0 1	C'_1=1
5	0 0 0 0 1 0 1	C'_1=0
6	0 0 0 0 0 1 1	C'_1=0

Figure 2. Equivalent OR gate with equal parity fan-out in testing mode 2.

The equivalent AND gate in testing mode 1 is displayed in figure 1.b, while the procedure to generate the universal and minimal test in testing mode 1 is described in table 2. The $T_{d\&}$ diagnostics test for the singular ≡1 constant defect in the maximally degenerated AND structure with 1 fan-out will contain $T_{d\&} = n$ stimulus arrays.

In a similar fashion, in testing mode 2, the $T_{d\vee}$ test generated by considering the characteristics of reconfiguring in a maximally degenerated OR structure (fig. 2), and in order to ensure the test's universality, will contain $T_{d\vee} = n$ stimulus arrays. The test diagnosis the singular ≡0 fault on the connections of an AND gate with one fan-out.

In general, the T_d diagnosis test which identified the singular constant defect ≡0 or ≡1 for a CC with r supplementary propagation paths with equal parity for the fan-outs will contain T_d stimulus arrays:

$$T_d = 2\cdot(n+r) \tag{5}$$

Furthermore, the T_c control test which checks for the lack of the singular constant defect ≡0 or ≡1 on the primary inputs of the CC with fan-outs with equal parity for the convergent signals will contain, regardless of the number of primary inputs two extraordinary sets – 11...1 and 00...1.

Analyzing the influence of the c connection fan-out over the procedure which generates the diagnosis test for CC with equal parity for the convergent fan-out allows us to highlight the following characteristics:

1) The test structures remains unchanged – the same "0" in field of "1" and "1" in field of "0"
2) Each fan-out diagnosis requires 2r extra stimulus arrays and an extra ESCP;
3) ESCP will be enabled only when opposite parities for the fan-out connection signals must be supplied artificially. This means C'=1
4) ESCP will stay disabled in all situations when the c^1 and c^2 signal parities must remain equal, as stated in the requirements for test universality. This means that C' = 0.

From the way an universal and minimal test is generated, the following conclusion can be drawn: when using a fan-out with equal parities and a single auxiliary path for the convergent signal propagation, creating the diagnostic test requires adding a ESCP on the extra primary input connection. The ESCP will be enabled only in order to achieve the opposite values – 10, 01- of the convergent signal.

Universal diagnostics tests synthesis for CC with opposite parities

Consider the Karnaugh diagram (table 4) which represents the Boolean function y_{po} with opposite parities for the fan-out signals (fig. 4,a):

$$y_{po} = a\cdot b\cdot c\vee\bar{c}\cdot d\cdot e \tag{6}$$

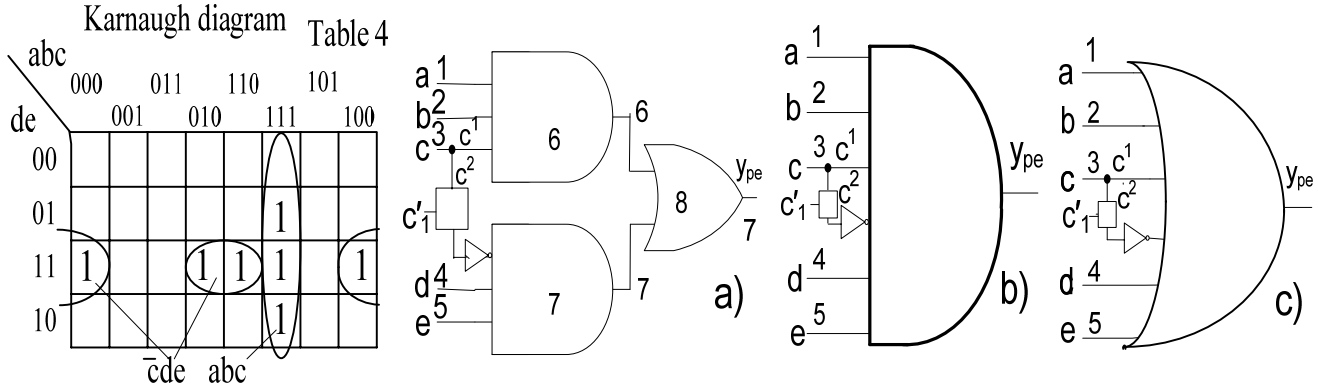


Figure 3. Repetitive CC with opposite parity (a) and the equivalent gates in testing modes 1 (b) and 2.

Tests of equivalent gate AND Table 5

No. test	Binary signals a b c^1 c^2 d e y_{pe}	Activation ESCP in testing mode 1
1	0 1 1 1 1 1 0	C'_1=0
2	1 0 1 1 1 1 0	C'_1=0
3	1 1 0 1 1 1 0	C'_1=1
4	1 1 1 0 1 1 0	C'_1=1
5	1 1 1 1 0 1 0	C'_1=0
6	1 1 1 1 1 0 0	C'_1=0

Tests of equivalent gate OR Table 6

No. test	Binary signals a b c^1 c^2 d e y_{pe}	Activation ESCP in testing mode 1
1	1 0 0 0 0 0 1	C'_1=0
2	0 1 0 0 0 0 1	C'_1=0
3	0 0 1 0 0 0 1	C'_1=1
4	0 0 0 1 0 0 1	C'_1=1
5	0 0 0 0 1 0 1	C'_1=0
6	0 0 0 0 0 1 1	C'_1=0

The AND gate, functionally equivalent with a maximally degenerated AND gate in testing mode 1 is described in figure 3,b. The universal test used to diagnose of the AND gate is described in table 5.

Analyzing the characteristics of the universal and minimal $T_{d\&}$ test for figure 3,b generation, we reach the following conclusion: for a single fan-out of the primary input with opposite parities for the convergent signals, in order to obtain the universal and minimal $T_{d\&}$ test, an extra ESCP must be added to the extra connection. The ESCP will be enabled, so that it will enhance homogeneity and allow obtaining a maximally degenerated AND circuit equivalent with the respective AND gate.

In testing mode 2, synthesis of the universal and minimal test T_{dv} to diagnose DC ≡0, ≡1 for the connections of the respective maximally degenerated OR structure will be done in the same manner, and the number of tests will be the same as in (6) and (7).

Design for testability of a repetitive CC with multiple inputs

Consider the repetitive CC in figure 4,a which contains both fan-outs with equal parities and fan-outs with opposite parities. Designing for testability of this CC by using a single CREDS and 2 ESCP [6] leads to the structure un figure 4,b, which in testing mode 1 will have to be reconfigured in a maximally degenerated AND structure equivalent to the AND gate, and the universal and minimal diagnosis test for the singular fault ≡0 will contain 31+2=33 stimulus arrays: 31 stimulus arrays for diagnosing the CC in 4,b without fan-outs and one stimulus array for each of the defects on connections 10_2 and 20^2 .

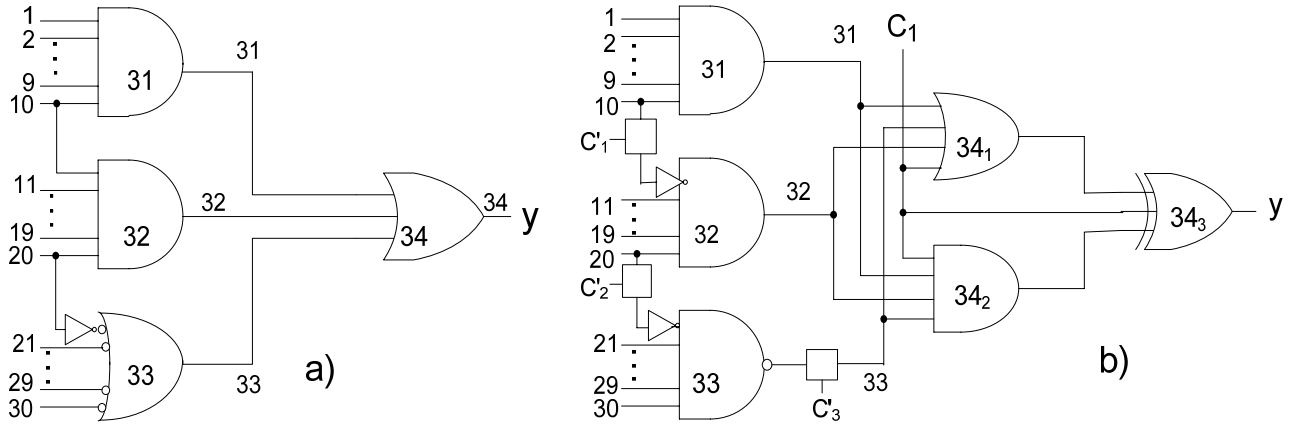


Figure 4. CC with multiple inputs with convergent fan-outs (a) and the structure obtained conform to DFT (b).

The DFT algorithm for the initial CC in figure 4.a is as follows:

1^0. Count all connections and gates in circuit 4.a, starting with the primary inputs, and arrange the elements on levels.

2^0. Place one ESCP (C^1 and C^2) on the 10^2 and 20^2 connections. (Fig. 4,b);

3^0. Analyze starting with level I and add a CESP on the connection – where needed – to extra reverse the signal on the desired connection (33) (fig 6,b)

4°. Analyze the types of the gates starting with level I, and when it is necessary to maintain functional circuit equivalence, add an ESCP (C_1^3) on the connection, to extra reverse the signal on the desired connection (33) (fig. 4,b);

5^0. Replace within the PPT gate 34 with the respective SDERC in order to minimize cost

6^0. To obtain the universal and minimal diagnosis test "0" in field of "1", change the stimulus array structure so that it will contain the (10^2, 20^2) fan-out connections, whose diagnosis will require extra stimulus arrays (12 and 22, marked with * in table 7). The order in which the tests are conceived is in table 7.

7^0. For the general PPT case (when all gates – 31, 32, 33 and 34 are replaced by CREDS), synthesis of the universal and minimal test for "1" in field of "0", change the stimulus array structure so that it will contain the (10^2, 20^2) fan-out connections, whose diagnosis will require extra stimulus arrays (12 and 22, marked with * in table 8). The order in which the tests are conceived is in table 8.

Table 7

Test No	Binary signals for the stimulus arrays															
	1	2	…	9	10^1	10^2	11	…	19	20^1	20^2	21	…	30	ESCP enabling in testing mode 1	
…	.	.	…	.	.	.	.	…	.	.	.	.	…	.	…	C_1^3=1
11	0	0	…	0	1	0	0	…	0	0	0	0	…	0	C_1^1=1; C_1^2=1	
12*	0	0	…	0	0	1	0	…	0	0	0	0	…	0	C_1^1=1; C_1^2=1	
.	.	.	…	.	.	.	.	…	.	.	.	.	…	.	…	
21	0	0	…	0		0	0	…	0	1	0	0	…	0	C_1^1=0; C_1^2=0	
22*	0	0	…	0	0	0	0	…	0	0	1	0	…	0	C_1^1=0; C_1^2=0	
…	.	.	…	.	.	.	.	…	.	.	.	.	…	.	…	

In table 7 we can notice that, for the stimulus arrays 11 and 12's sets, the binary values for the 10^1 and 10^2 signal connections must be opposite, therefore $C_1^2 = 1$. In the same time, on the 20^1 and 20^2 connections a "1" binary value must be ensured. As such, $C_1^2 = 1$.

On the contrary, for the 21 and 22 stimulus arrays, the binary values for the 20^1 and 20^2signals must conform to the "0" in "1" field as universal test requests, that is to be opposite, and such $C_1^2 = 1$. Because of the same hypothesis as above, the binary values for 10^1 and 10^2 must equal 1. This requires that $C_1^1=0$.

Table 8.

Test No	Binary signals for the stimulus arrays															
	1	2	…	9	10^1	10^2	11	…	19	20^1	20^2	21	…	30	ESCP enabling in testing mode 1	
…	.	.	…	.	.	.	.	…	.	.	.	.	…	.	…	$C_1^3=1$
11	0	0	…	0	1	0	0	…	0	0	0	0	…	0	$C_1^1=1$; $C_1^2=1$	
12*	0	0	…	0	0	1	0	…	0	0	0	0	…	0	$C_1^1=1$; $C_1^2=1$	
.	.	.	…	.	.	.	.	…	.	.	.	.	…	.	…	
21	0	0	…	0		0	0	…	0	1	0	0	…	0	$C_1^1=0$; $C_1^2=0$	
22*	0	0	…	0	0	0	0	…	0	0	1	0	…	0	$C_1^1=0$; $C_1^2=0$	
…	.	.	…	.	.	.	.	…	.	.	.	.	…	.	…	

The synthesis procedure for the universal and minimal diagnosis test for the maximally degenerated structure OR will be executed by considering the same hypothesis. In this case the number of stimulus arrays will be $T_{dv} = n+2$ stimulus arrays, same as for the universal "0" in "1" field universal test for the maximally degenerated AND test: $T_{d\&} = n+2$ stimulus arrays. Thus, in this situation, the universal and minimal diagnosis test will contain $T_d = 2(n+2)$ stimulus arrays.

Conclusions

Designing for testability by using CREDS and ECSP allows diagnosing any internal connection of a repetitive CC and can be a good starting point to enhance testability for digital structures while establishing the fabrication process. Diagnosing DC ≡ 0, ≡ 1 for each supplementary path connections for the fan-out requires 2 extra stimulus arrays. The ECSP enabling restrictions C_1^1 , C_1^2 and C_1^3 are the same in both testing modes.

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