A Review of ESD Stress Models

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Abstract—**This paper presents the fundamental types of ESD phenomenon and the basic ESD stress models with their test methods characteristics concerning the IC (Integrated Circuits). The ESD models define how semiconductor devices are to be tested for ESD sensitivity under different working conditions and the procedure of classifying microcircuits according to their susceptibility to damage by exposure to electrostatic discharge (ESD). The resulted classification is used for establishing appropriate handling requirements in accordance with international standards.**

Index Terms—**electrostatic discharges, susceptibility, stress measurement, sensitivity, standards**

I. INTRODUCTION

ESD occurs when an electrostatic voltage slowly develops between an object and its surrounding environment. In IC environment there are a multitude of processes that may generate charge from persons or objects, such as modules, ICs, parts of machines, packages and even CRT screens.

The electrostatic voltage resulting from the separation of charge is the driving force for the discharge current. The voltage on a charged object relative to earth ground can be measured by means of an electrostatic voltmeter. If a discharge takes place between two objects, then the voltage difference and the capacitance between the objects must be considered at the actual instant of discharge. Decreasing the distance between the objects or adding the third object at a lower potential, increases the capacitance and reduces the voltage. This phenomenon is known as capacitive voltage suppression. [1]

Electrostatic discharge occurs in a variety of ways, depending on how the static charge is accumulated and how the charge build-up is dissipated. At this moment, there are three standard ESD models [1, 2, 3, 4] defining how semiconductor devices are to be tested for ESD sensitivity under different situations of electrostatic built-up and discharge.

Electrostatic charge build-up is the result of an imbalance of electrons on a material surface. This charge build-up develops an electric field that has measurable effects on other objects at a distance. The process of electron transfer as a result of two objects coming into contact with each other and then separating is known as triboelectric charging [1]. The prefix “tribo” means “to rub”. The charging process results in one object gaining electrons on its surface and then becoming negatively charged, and another object losing electrons from its surface and therefore becoming positively charged.

Even a person can get triboelectrically charged, just by walking. Thus, some materials become negative charged and other positive and this depends of relative tendencies of materials that lose or gain electrons. These tendencies are described in Triboelectric series – a list of various materials and their tendency to gain or lose electrons. [5]

II. ESD STRESS MODELS

In an IC environment, there are two fundamental types of ESD phenomenon occurred and simplified into "stress models". The first type implies a person charged either to a positive or negative potential relative to the ground, approaching a grounded IC (Integrated Circuit) that is at other potential. When the air brakes down between the finger and one pin of the IC, the protection structure in the IC turn on and the capacitance of the body is discharged via the IC and the grounded pin into the ground. Without the protection we can obtain unwanted results causing the IC damage.

The model described, known as the HBM (Human Body Model), is a very commonly used model for testing the sensitivity of a device to ESD [1] (figure 1).

The second model type is the MM (Machine Model) a model introduced in Japan as a more severe HBM with a 0 Ω discharge resistor and a larger capacitance. As a result of investigating the worst case scenario of the HBM model, the MM simulates a more rapid electrostatic discharge from a charged machine, tool or fixture. The appropriate test circuit consists of a 200 pF capacitor charged to a certain voltage and then discharging this capacitor directly into the device being tested through a 500 mH inductor (figure 2).

The third model of ESD is the electrostatic discharge from a charged device to another device. This can be more destructive than HBM ESD because of its high current. The charge transfer from an ESD device is also an ESD event. A device may become charged from sliding down the feeder in an automated assembler. If it then enters in contact with a conductive surface, a rapid discharge may occur from the device to the metal object. This model is known as the Charged Device Model (CDM) and can be the most destructive than any other events.

The characteristics of the three basic ESD models are described below:

The first ESD model is called **HBM (Human Body Model).**

This model dates back to the 1800s and first gained acceptance in the semiconductor industry in the late 1960s as a method for simulating failures of JFETs (Junction Field Effect Transistor) used in the Flight Control Computer for the United States Titan III Space Program [1].

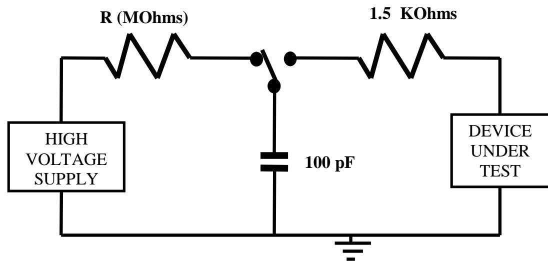

Figure 1. The Human Body Model.

The model has a 100 pF capacitor that discharges through a 1.5 kΩ resistor and a switch to the device under test (DUT). There are two types of HBM standards. The first defines the ESD withstand level for IC components susceptibility and the second was developed to define the potential levels of exposure to products and any systems by users through either in contact or by air discharge. IEC 61000-4-2 presents the second HBM ESD standard. This is an immunity standard and its objective is to determine the susceptibility of products or systems to the HBM electrostatic discharge.

Concerning the IEC 61000-4-2 standard, its original edition was known as IEC 801-2 1984 and later became IEC 1000-4-2. Once approved by the IEC and adopted by the European Commission, this standard became EN 61000-4-2.

The second ESD model is the **MM (Machine Model).** Standards that define the MM ESD testing are JDEC's JESD22-A115 and ESD Association's ESD STM5.2: Electrostatic Discharge Sensitivity Testing - Machine Model. This model has a 200 pF capacitor and the 1.5 kΩ resistor is replaced with a 0.5 µH inductance.

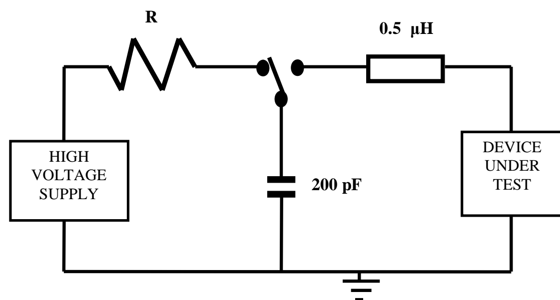

Figure 2. The Machine Model.

The Machine Model (MM) was intended by Japanese IC manufacturers as a more severe HMB model. The capacitance is defined as 200 pF, while the resistance R_{MM} is zero (in a real ESD tester the resistance will be greater than zero). ESD associations and standardization organizations have improved the correlation of this model with HBM by defining a discharge current waveform that implies an effective inductance of 0.75 µH and an effective resistance of 10 Ω in the discharge part [3]. It is known that the effective inductance in earlier specifications was 0.5 µH.

The **CDM** (**Charged Device Model**) is the third ESD model. CDM is characterized by a rapid energy discharge from a conductive body onto an ESD device. The duration of the discharge is very short - usually less than one nanosecond. The peak current can reach several tens of amperes. Many test methods have been tested to reproduce the real-world CDM event and provide a suitable test method that duplicates the types of failure that have been observed in CDM caused circuit failures.

There are two separated CDM test methods. The first one, named RCDM (Real world event CDM), best replicates the real world charged device event. The second one addresses devices that are inserted in a socket and then charged and discharged in that socket [4]. It is named socketed discharge model (SDM). SDM simulates a device inserted in a socket and charged from a high voltage source and then discharged through a 1-ohm resistor. SDM is easy to reproduce in laboratory but is not always replicating the real life CDM ESD events. The international standard for CDM testing is ESD-STM5.3.1: Electrostatic Discharge Sensitivity Testing - Charged Device Model (published in 1999) [6].

This standard establishes the procedure for testing, evaluating and classifying the electrostatic discharge (ESD) sensitivity of components to a defined charged device model (CDM). Corresponding to this standard, the ESD sensitive components are classified according to their ESD withstand voltage using the test procedure described in the standard.

The CDM ESD component classification levels are shown in the table below:

TABLE 1. THE ESD COMPONENT CLASSIFICATION LEVELS [6]

CLASS	VOLTAGE Range
C1	<125 v
C2	125 v to <=250 v
C3	250 v to <= 500 v
C4	500 v to <= 1000 v
C5	1000 v to <= 1500 v
C6	1500 v to <= 2000 v
C7	=>2000 v

The specific charging and discharging methods for the CMD model are described below.

Charging methods:

- Direct charging method: the component to be tested is placed on the ground plate with its leads pointing up, then charging it (and discharging the device) [5]. A typical CDM test circuit is shown below:

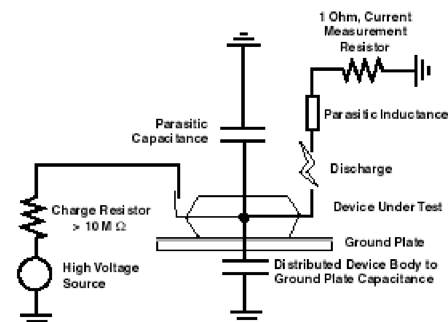

Figure 3. Typical CDM test circuit.

According to the ESD-STM5.3.1 [6] standard, the total charging resistance shall be at least 100 megohms. The component is charged trough the pin which best provides a connection to the substrate or bulk material of the component.

- Field induced method: the component to be tested is placed on the charging plate and then the potential of the component is raised by energizing the field charging plate. Discharge is made through all the pins, including Vcc and Vss, one at time [6].

Discharging methods:

- Non-contact mode discharge: Air discharge attempts to simulate the CDM event as it naturally occurs in the environment. The discharge occurs across a small air gap. The discharge will vary depending upon a number of factors that are difficult to control, such as air pressure, humidity etc. These tend to alter the discharge characteristics, making replication in a real test environment very difficult to reproduce. The major advantages of the non-contact mode discharge technique are that it truly represents the natural discharge conditions and minimizes the parasitic circuit elements. The major disadvantages are an inability to ensure discharges to a chosen pin when testing devices with very close pin spacing and difficulty in reproducing the discharge events within close tolerances.

- Contact mode discharge: the contact mode simulates the ESD event in a way that is really repeatable. However, the actual current waveforms obtained are different from the non-contact mode waveforms [4]. A major advantage of contact mode testing is repeatability of the test on a given tester and the ability to more easily test devices with fine lead pitch. According to the ESD-STM5.3.1 standard the major disadvantage of the contact mode testing is that, parasitic elements significantly influence the discharge current waveforms [6].

The CDM either with direct or with field-induced charging is the most frequent discharge mechanism in an automated handling environment. The schematic of the first CDM-test setup was developed by P.R. Bossard [7]. The configuration describes the contact mode method (because of the used relays). The device was lying in "Dead Bug" position on a ground plane to achieve a well-defined, large capacitance and connected with a charge relay and a discharge relay, as shown in the figure below:

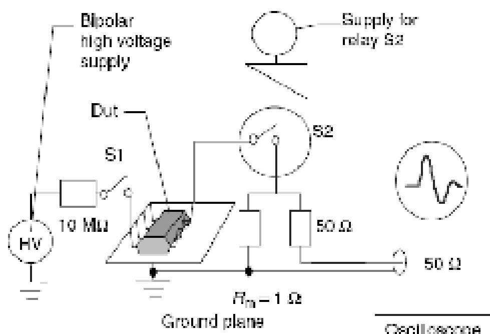

Figure 4. The first CDM test system (P.R. Bossard).

The "charge pin" is the pin with the best contact to the substrate and the capacitance between the lead frame with the chip and the ground plane was charged via one pin and discharged via another pin. The capacitance of the device to ground depends on the package and on any air gap or other dielectric between the package and the ground plane. As described in [1, 8, 9], the actual voltage is determined by the resistance of the voltage source and the isolation resistance between the chip and the ground plane.

For running the test, the IC is fixed by vacuum in “Dead Bug” position on a charge plate. The charge plate can be alternatively switched to a high voltage or to ground via a high value resistor. Four procedures of (F)CDM - charging and stress can be found implemented in the different testers. It should be noted that the thresholds failure depends strongly on the polarity of the stress current. For analysis purposes it is important to know the thresholds for both polarities and the associated failure sites.

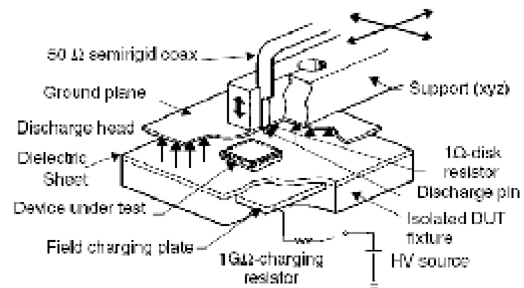

Figure 5. FCDM test system with disk resistor.

The ESD Susceptibility Symbol used to identify ESD sensitive circuits is shown in figure below:

Figure 6. ESD Susceptibility Symbol.

The ESD testing models can be implemented with algorithms and techniques of CAD simulation [10, 11, 12] using appropriate programs, like SPICE or PSPICE. The results consist in comparison of currents or I-U characteristics and can lead to a very good accuracy concerning the implementing of ESD models.

III. A QUANTITATIVE EVALUATION

Concerning the quantitative evaluation of the performances of all general electrical and electronic equipments for ESD immunity, we need an ESD test generator that should meet the requirements of EN 61000-4-2 immunity standard. The ESD generator shall provide the specific voltage levels (defined for each peak current value) for equipments immunity test. The waveform of the ESD generator for ESD testing output current must be as described in EN 61000-4-2 standard:

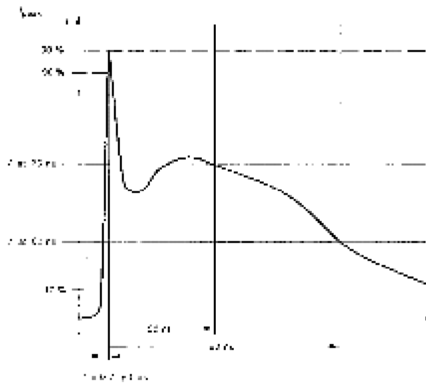

Figure 7. The ESD test generator output current waveform.

We should obtain the same current waveform at all voltage levels when discharge method is used.

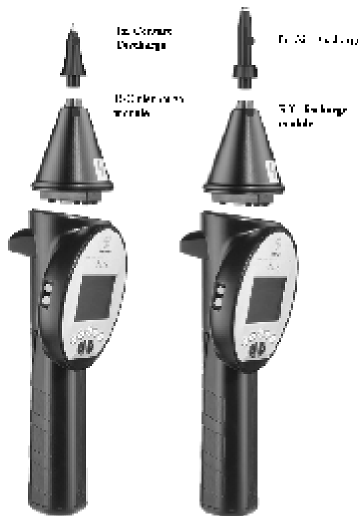

Figure 8. The compact **dito** ESD simulator.

An example of an ESD generator we use in our laboratory for ESD test is shown in the figure 8. It generates ESD pulses up to 16 KV in air discharge and 10 KV in contact discharge.

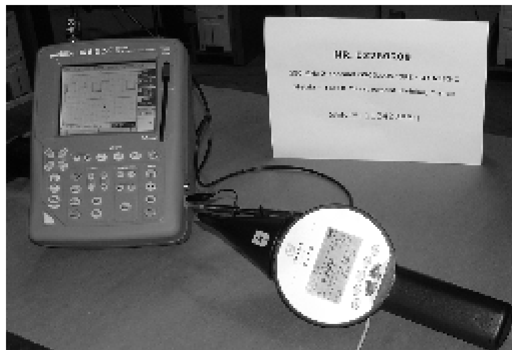

Figure 9. Photo from an ESD test using **dito** ESD simulator.

During the immunity tests (figure 9), all parameters are stored into an internal non-volatile memory and by connecting the device to a computer, all data sets from tests could be uploaded. Air discharges can imply significant variability from discharge to discharge, particularly above 4 kV. For this reason and for assuring the test repeatability, the IEC 61000-4-2 test standard accentuates the contact discharge method and recommends the air discharge method for use only if no metal parts are exposed.

IV. CONCLUSIONS

The fundamentals of the basic ESD stress models and their specific test methods are important for circuit protection and evaluation of integrated circuits susceptibility at electrostatic discharges. Considering that electrostatic discharges occur in any environment where charged objects may come in contact with each other and that the voltage discharge that takes place can cause serious damages in ICs environments, the importance of ESD and its following events has significant grown. We presented the three ESD models and a quantitative evaluation of the EN 61000-4-2 standard.

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