Research of Impulse Heat Resistance of Powerful Switching DMOS Transistors

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Abstract—Heat resistance of powerful switching transistors of DMOS-structures (a metal-oxide-semiconductor structure, formed by a double diffusion method) has been researched. It has been determined, that both impulse characteristics and heat characteristics of the device, to which we should ascribe crystal heat capacity and heat conduction, influence impulse resistance value. The obtained dependences of the relation of heat resistance in static mode on control impulse duration at different filling factors allow to determine the impulse heat resistance value and the area of safe operation of the devices of this class.

***Index Terms*—filling factor, heat conduction, heat resistance, impulse, powerful switching DMOS-transistor**

I. INTRODUCTION

The dependence of impulse heat resistance on the impulse duration and on the filling factor of the impulse pattern for field-effect transistor КП 921 has been determined.

The maximum dissipated power of a transistor, working in a switching mode, consists of structure resistance loss, switching loss and control in the gate circuit loss.

Power loss in the gate circuit is much less than the loss, defined by the open structure resistance, i.e. the loss, caused by the final conduction magnitude of a transistor in an on condition, makes a dominant contribution to dissipated power.

The transistor under study has the following parameters:

Maximum drain current $I_{D.\max} = 10A$. Drain-source breakdown voltage $U_{DS.break} = 50-60V$. Threshold voltage $U_{thr} = 3-5V$.

A copper radiator, to which the transistor under study was attached (through heat-conducting layer BeO_2) was used for withdrawal of heat, evolving on the resistance of an open structure. In static mode the maximum permissible power, dissipated on the transistor, is determined by a relation [1]

$$P_{\max.st.} = \left(T_{cr.\max.} - T_{body}\right)/R_{T.st.}, \qquad (1)$$

where $T_{cr.\max.}$ – maximum temperature of the crystal (for silicon structures it makes $130^o C$), T_{body} – temperature of the transistor body, $R_{T.st.}$ – heat resistance in static mode.

Heat resistance of the devices under study made $R_{T.st.} \approx 1.1^o C/W$.

The area of safe operation is limited by a maximum permissible operating drain current, drain-source breakdown voltage, maximum dissipated power [2, 3].

The area of safe operation of a powerful field-effect transistor was defined by the change of I_D, stipulated by crystal heating. In static mode, the maximum dissipated power made $40-50W$.

Unlike static mode of operation, inertia of thermal processes, stipulated by heat capacity and heat conduction of the crystal, will influence its temperature in an impulse mode of operation. Therefore, it will depend on both average value of power, brought to the device, and time-frequency impulse pattern. Squared shape impulses were used in the process of impulse heat resistance study.

Instantaneous value of crystal temperature increases towards the end of each impulse action and dicreases towards the beginning of the next one. Deviations of crystal temperature from average value are determined by the relations between the impulse t_1 duration and a structure heat time constant and also by duration of the time interval between the impulses t_2 and a cooling time constant.

It is expedient to use the notion of impulse resistance $R_{T.imp.}$ in the process of transistor's operation in a switching mode.

The maximum permissible impulse power, dissipated by the transistor, is the following

$$P_{\max.imp.} = I_{D.imp.} \cdot U_{DS.imp} = \left(T_{cr.\max.imp.} - T_{body}\right)/R_{T.imp.}, \qquad (2)$$

where $I_{D.imp.}$ – impulse drain current, $U_{DS.imp.}$ – impulse drain-source voltage.

At experimental determination of $R_{T.imp.}$ not a time-averaged structure temperature but its maximum level in an impulse mode $T_{cr.\max.imp.}$ is taken into consideration.

In the process of research, the body temperature was kept on the level of $25^0 C$ due to the air blow-off of the copper radiator, and was controlled with the help of thermocouple.

Instantaneous temperature of the crystal was defined according to the drain current value, measured in the intervals between the operating impulses. The current value made ~ $1мА$ at indoor temperature and it did not influence the self-heating process of the structure in the intervals between the impulses.

The current impulse values, conditioning self-heating of the structure, were specified by signal amplitude quantity at the outlet of impulse generator and were controlled by voltage drop on linear load in the drain circuit. The control of drain current, flowing through the structure during the intervals between the impulses, was realized by drop voltage on nonlinear load, also connected to the drain circuit. It has a large resistance for small drain currents and large conduction for large impulse currents.

In order to determine the maximum permissible dissipated power, the dependence of $R_{T.imp.}/R_{T.st.}$ on impulse duration and filling factor, shown at fig. 1. for the transistor under

study, is used.

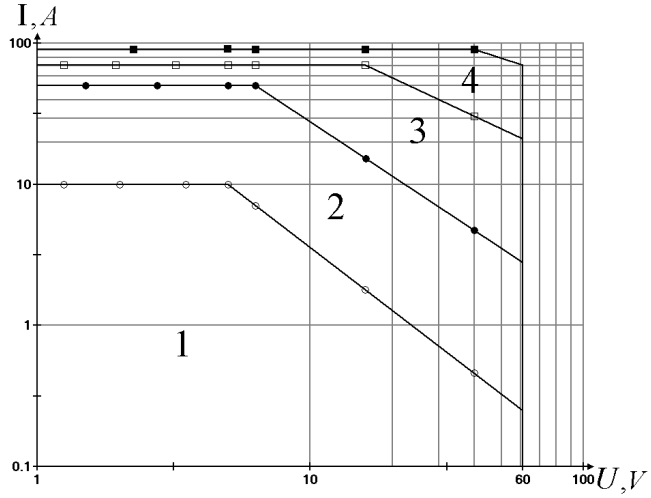

Fig. 1. Areas of safe operation of a powerful switching transistor КП 921 in static and impulse modes:
1-static mode (○ - limits of area 1);
2-impulse mode $t = 50\,mcs, D = 0{,}5$ *(● - limits of area 2);*
3-impulse mode $t = 50\,mcs, D = 0{,}2$ *(□ - limits of area 3);*
4-impulse mode $t = 50\,mcs, D = 0{,}01$ *(■ - limits of area 4);*

Using the dependences of $R_{T.imp.} / R_{T.st.}$ on impulse duration and filling factors with consideration of (2), it is possible to define the maximum permissible dissipated power for any values of filling factor and impulse duration.

While working with short duration impulses and a small filling factor of impulse response $(t_1 = 10...50\ mcs,\ D = 0{,}01)$, the area of safe operation in the coordinates $\lg I_{DS.imp.} - \lg U_{DS}$ has practically a rectangular shape (fig.2.)

The maximum drain current reached $90\,A$.

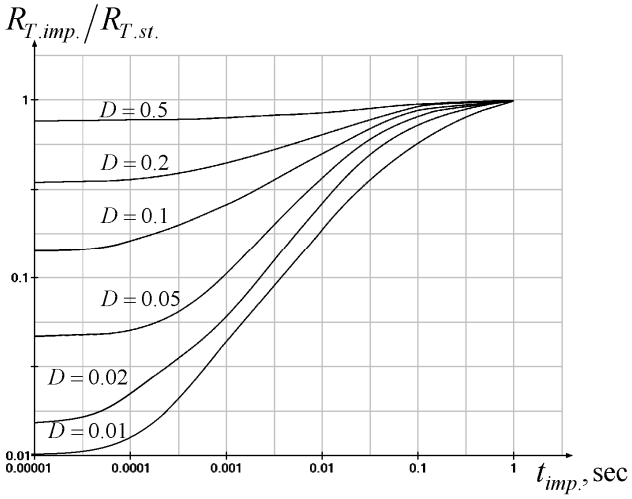

Fig. 2. Dependences of $R_{T.imp.} / R_{T.st.}$ *on impulse duration* $t_{imp.}$ *at different filling factors.*

For the transistor under study, the area of safe operation in an impulse mode (at $t_1 = 10\,mcs,\ D = 0{,}01$) is defined by the maximum impulse current of $90\,A$, maximum drain-source voltage of $60V$ and dissipated power of ~ $6\,kw$.

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